Pianocorder™* reproducing system / marantz™* reproducing piano

CIRCUIT DESCRIPTION AND SCHEMATIC DIAGRAMS

FOR MODEL NUMBERS P-100, P-100M, P-101, P-101M, P-200, PR-200, PR-201

FOR USE BY QUALIFIED TECHNICIANS ONLY

Pianocorder™ reproducing system / marantz™ reproducing piano

CIRCUIT DESCRIPTION AND SCHEMATIC PACKAGE

* PIANOCORDER is a trademark owned by Superscope, Inc. for its reproducing systems and components--protected under U.S. Patent Numbers: 3,905,267; 3,604,299; 4,031,706; 4,104,950; 4,121,491; 4,132,141; 4,132,142; 4,135,428; 4,161,901, and other U.S. and foreign patents pending.

PIANOCORDER
CIRCUIT DESCRIPTION
TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

INDEX OF

FIGURES, DIAGRAMS AND TABLES

INDEX OF

FIGURES, DIAGRAMS AND TABLES

INDEX OF

FIGURES, DIAGRAMS AND TABLES

I. SYSTEMS DESCRIPTIONS

A. P-100, P-100M

The P-100 and P-100M PIANOCORDER Reproducing Systems can be separated into three major components: the power supply, the recording system and the reproduction or playback system. The P-100 is the kit form installed by an independent technician. The P-100M is the P-100 system installed and factory adjusted in the MARANTZ* Reproducing Piano.

The function of the power supply is to transform the AC mains power supply into the three DC voltages required by the system to operate. The record system assembles the pedals and notes played and the expression or loudness with which they are played into a continuous sequence of digital data signals. These data signals are recorded on a standard Phillips type cassette travelling at 3 3/4 ips (9.5 cms) creating a permanent record, in digital form, of the musical performance. Reproduction of the performance is accomplished in this manner: the recorded cassette is started at the beginning of the recorded material and reproduces a signal which represents the data assembled during recording. The signal is supplied to the playback board where it is decoded into the following components: sync word, notes, pedals, expression and control bits. The notes are transferred to the individual driver boards and thus to the individual note solenoids. The expression is also transferred to the driver boards and controls the force with which the hammer strikes the strings. The pedals are also operated precisely at the time in the passage when they were recorded. Thus not only are the notes reproduced, but also the precise expression of the artist is created, thus generating the subtle tone colors possible with the pianoforte.

B. P-101, P-101M

The P-101 and P-101M PIANOCORDER Reproducing System is the playback only version of the basic P-100 system. Thus, this model consists of the cassette reproducer, the playback decoder and the note and pedal mechanism noted above as well as the power supply. The ability of this system to reproduce musical passage is identical to that of the P-100 system. The P-101M is the playback only system factory installed and adjusted in a MARANTZ Reproducing Piano.

C. P-200

The P-200, also referred to as the vorsetzer system, is essentially the same system as the P-101 with the exception that it is fitted in a stylish cabinet (available in several cabinet finishes) which allows it to be attached to the

*MARANTZ is a trademark owned by Superscope, Inc. for its reproducing systems and components.

piano or removed at the discretion of the user. Note that the P-100 and 101 systems above are mounted inside of the piano and are concealed by the cabinet.

D. PR-200

The PR-200 consists of the recording system of the P-100 and an extension cable. This unit can be installed in any piano and is used in conjunction with the P-200 to allow the user to record his performance on the cassette recorder reproducer housed in the P-200 (vorsetzer).

E. PR-201

The PR-201 is similar to the PR-200 but is intended for use with the P-101 to enable it to record also. Thus, the P-101 and the PR-201 comprise the same system as the P-100.

II. POWER SUPPLY

A. General Description

The power supply transforms the AC mains power into the three DC voltages required for operation of the system. These voltages are: 170 Volts DC for operation of the note and pedal solenoids; 12 Volts DC for operation of the record board, the tape recorder and a portion of the playback board; 5 Volts DC for operation of the playback and driver boards and control circuits contained in the tape recorder.

B. Generation of 170 Volts DC

The line cord of the system is connected to the wall socket which must provide between 105 and 125 Volts AC, 50 to 60 Hz, with a minimum of 15 amperes. This voltage is connected to SW2, the safety interlock switch, mounted behind the lower frame panel on the piano. This switch is a three position switch with one position momentarily on (when pushed in) center off and locked on (when pulled out). This switch disconnects power when the lower panel is removed until the switch is deliberately pushed in or pulled out. This feature minimizes accidental shock hazard to service personnel. AC mains power is connected to the power supply at J 6 Pins 1 and 3. The active line coming in on Pin 1 is directed through FS 1, a 12 amp ceramic fuse, and connected to J 5 Pin 4. The neutral line coming in on Pin 3 of J 6 is connected directly to Pin 2 of J 5. AC mains power leaves the playback board on J 5 Pins 2 and 4 and is connected to SW1, the power switch, located on the left hand side of the tape recorder bracket. When closed in the on position, power is returned to the power supply on J 5 Pins 1 and 3 where it is distributed to two places. First, it is applied across RV 1. RV 1 is a metal oxide varistor (m.o.v.). The useful characteristics of this component are that it presents a low impedance to transients, spikes or noise voltages and a high impedance to normal voltage and frequency components. Thus, transients generated outside the unit by, for example, an electric motor will be reduced an appreciable amount so that it does not interfere with normal operation of the power supplies and thus the rest of the system.

POWER SUPPLY

117 Volts AC, nominal, is applied to a full wave bridge rectifier consisting of D 8, 9, 10 and 11. Thus a DC potential of approximately 170 volts is produced between the junctions of D 8 and 10 and D 9 and 11 (refer to power supply schematic). RT1 is a thermistor whose useful characteristic is as follows: when power is first applied to the unit it presents a high impedance to the 170 Volt positive supply line. Were this element not present, the turn-on surge created by the unit could overload the circuit breaker or fuse supplying power to the PIANOCORDER unit. As the unit is playing and power is drawn through RT1 and it heats

up, the resistance decreases greatly. This thermistor has a cold resistance of several hundred ohms and a hot resistance of several tens of ohms. C 8 functions as a ripple filter, or reservoir capacitor. Since the 170 Volt supply line is not regulated, all filter of transients and ripple is supplied through the action of C 8. Its function is thus to stabilize the 170 Volt DC line. Since the 170 Volt line is not regulated, it will vary in potential with the voltage of the AC mains power applied. R 12 is a bleeder resistor whose function is to provide a low resistance discharge path to capacitor C 8 when power has been turned off. Were R 12 not present, C 8 would hold a lethal charge for several hours. With R 12 present, the voltage across C 8 is reduced to a non-hazardous 40 volts in approximately 60 seconds. The load on the 170 volt line is about 3.5 watts (21 ma) through R 12 when the unit is turned on but not playing. Average power when the piano is playing is between 300 and 400 watts (3 to 4 Amperes). Occasional power surges may draw 1000 Watts (9 Amperes). The 170 Volts DC present at J 2 Pins 1 and 2 is supplied to the driver board where it operates the note solenoids. The 170 Volts are also applied to FS 3 and FS 4. These fuses are in series with the Soft and Sustain Pedal solenoids to prevent damage to them due to failure of the drive components Q 7 and 8. Thus, it is seen that the 170 Volts DC is the operating power for all solenoids.

C. 12 Volt DC Supply

AC mains power is also applied through FS 2 (1.5 A) to terminals E1 and E2, the primary winding of transformer T1. Fuse FS 2 will open if an overload condition is produced in either of the secondary circuits. The secondary winding terminated at E3 and E4 steps down the primary voltage from 117 Volts AC to approximately 16 Volts AC which is applied to the full wave rectifier consisting of D 1, 2, 3 and 4 which produces a direct current potential across C 1 of about 25 volts. C 1 acts as C 8 did to stabilize the DC supply and reduce ripple. U 2 is a three terminal integrated circuit voltage regulator. Input is on Pin 1 and output is on Pin 2 and the common circuit connection is Pin 3. It is thermally connected to the power supply chassis which acts as a heat sink. Note that it is electrically isolated from the chassis. U 2 is a 12 volt regulator and the output voltage thus produced at J 1 Pins 5 and 6 is 12 Volts DC nominal. C 2 acts to stabilize the output voltage and reduce ripple as well as improve the transient response of the regulated voltage.

D. 5 Volt DC Supply

AC mains power of 110 Volts AC is also transformed across T 1 to the other secondary winding and terminated at

II. POWER SUPPLY (Cont)

E 5 and 6. The AC voltage present is approximately 10 Volts. DB 1 is another full wave bridge rectifier producing a DC voltage of approximately 15 volts across C 3. C 3 acts as C 1 and C 8 did to reduce ripple, etc.

The 5 volt supply is regulated through the action of Q 2, Q 1; resistors R 19, 1, 4, 8, 9, 6, 7; capacitors C 4, 7, 9; and integrated circuit U 1 (a 723 type precision voltage regulator). This circuit is a standard linear type series pass power supply regulator. The operation of the regulator is as follows. R 4, 8 and 9 form a voltage divider network across the regulated output voltage. The DC voltage on the wiper of variable resistor R 8 is applied to U 1 Pin 4 which is the inverting input to the comparison amplifier in U 1. The value of this voltage is weighed against the voltage present at Pin 5 of U 1 which is produced by the voltage divider action of R 6 and 7 from the reference voltage being provided at Pin 6 of U 1. Thus, if the output voltage tries to decrease, it produces an error voltage at the output of U 1, Pin 10, because the reference voltage has remained constant. This error voltage goes more positive which causes the collector emitter junction of Q 1 to decrease in voltage which in turn decreases the collector emitter voltage of Q 1 which increases the voltage present at the emitter of Q 2. In a similar manner, if the output voltage attempts to increase, the circuit operates in an inverse manner and causes the voltage present at the emitter of Q 2 to go lower. Thus precise voltage stability is maintained. R 19 serves to develop the voltage generated by Q 1 enough to turn on Q 2. C 4 operates in a manner similar to that of C 2 in the 12 volt supply section, to stabilize the output voltage and improve response of the regulator to transient voltages. C 7 serves to bypass noise on the non-inverting input of U 1 which is Pin 5. C 9 provides frequency compensation for U 1. D 6 and 7, and capacitors C 5 and 6 form a voltage doubler circuit. The voltage produced is used to supply operating voltage to U 1 independent of the input and output voltages of the 5 Volt supply.

E. GROUNDING

GROUNDING OF THE UNIT IS ACCOMPLISHED IN THE FOLLOWING MANNER. THE ROUND PIN ON THE THREE WIRE AC PLUG IS THE GROUND OR EARTH CONNECTION. IT IS CONNECTED TO A SEPARATE GROUND PLATE SECURED TO THE BOTTOM OF THE PIANO. ALSO SECURELY CONNECTED TO THIS PLATE ARE TWO OTHER GROUNDING WIRES. ONE OF THESE WIRES IS FIRMLY CONNECTED TO THE KEY SOLENOID RAIL. THE OTHER WIRE IS SECURED TO THE METAL FRAME (ALSO CALLED THE PLATE OR HARP FRAME) OF THE PIANO ON WHICH THE STRINGS ARE MOUNTED. THESE ARE THE ONLY PLACES THAT A GROUND IS PROVIDED. THUS, NOTE THAT NONE OF THE COMMON

II. POWER SUPPLY (Cont)

POINTS ON THE VARIOUS SUPPLY VOLTAGES IS CONNECTED TO THE GROUND. THUS, IT MUST ALWAYS BE REMEMBERED THAT CONNECTION OF A PIECE OF GROUNDED TEST EQUIPMENT TO ANY OF THE COMMON POINTS IN ANY OF THE POWER SUPPLIES CAUSES A DISASTROUS CONSEQUENCE TO THE CIRCUIT INVOLVED. THAT IS, ALL OF THE INTEGRATED CIRCUITS CAN BE INSTANTLY DESTROYED AS WELL AS A LETHAL SHOCK HAZARD MAY BE PRESENT TO THE SERVICE TECHNICIAN. THIS IS AN IMPORTANT POINT TO REMEMBER.

The remaining circuitry on the power supply board are the drive circuits for the soft and sustain pedals and will be discussed later.

III. RECORDING SYSTEM

A. Description

The recording system of the PIANOCORDER Reproducing System is an entirely digital serial word format. Switches beneath each of 80 keys on the keyboard as well as the two pedals, soft and sustain, are multiplexed into a 128 bit serial data frame. Notes 1-4: A, A#, B, C; and notes 85 - 88 A, A#, B, C are not included in the system because of the physical limitations the dimensions of the piano imposes on the PIANOCORDER system. Very few compositions will be affected by the exclusion of these eight notes. Expression or dynamic intensity is calculated and also introduced into this 128 bit word. The data thus produced is converted to a two tone or bi-phase signal which is supplied to the tape recorder and recorded onto a standard Phillips type cassette running at 3 3/4 ips (9.5 cms).

B. System Timing Generation

1. Clock Generation

All timing signals in the record board are derived from a master 9 kHz clock generator consisting of U 21 B and U 26 C and D, resistors R 56, 37, 39, 40, 41, 42, variable resistor R 38 and capacitor C 17. The four requirements for signal generation are: a power source, a frequency determining device, an amplifier with gain, and positive feedback. Frequency of operation is determined by C 17, R 56 and R 38. Thus, varying R 38 will change the frequency of operation. This control is precisely calibrated and sealed at the factory and should never need adjustment. R 39 and 40 provide proper bias for U 21 B, and positive feedback for U 21 B. R 41 isolates the output of the multivibrator and the input of U 26 D. R 37 isolates the input of U 21 B from the frequency determining components. Inverter U 26 D provides output drive and isolation for the 2 X CLOCK signal. R 42 provides positive feedback for snap action to improve the transition times of the output. The output of U 26 C is the inverted 2 X CLOCK which is used to clock the bass and treble expression counters, the operation of which will be described later. The CLOCK frequency is derived from pin 1 of U 11 A. U 11 A is a J-K flip-flop whose purpose is to act as a frequency divider to provide the clock signal to all necessary points. The clock signal is distributed to the following points:

TABLE 7
CLOCK DISTRIBUTION AND FUNCTION

Location	Function
U 19 Pin 1	Bi-Phase Converter
U 12 Pin 2	Clocking of frame delay and double registers
U 20 Pin 2	" " " " " "
U 25 Pin 2	" " " " " "
U 29 Pin 2	" " " " " "
U 8 Pin 3	Clocking for Parallel-in Serial-Out Expression converter shift registers
U 23 Pin 8	" " " " " "
U 24 Pin 5	Clocking for Key counters
U 23 Pin 5	" " " " "
U 2 Pin 1	Input to clock divider

2. Clock Division

U 2 is the master clock divider. The clock frequency, a 4.5 kHz (222 msec) symmetrical square wave, is applied to Pin 1 and is divided down into the following frequencies:

TABLE 8
CLOCK DIVISION FREQUENCIES AND TIMES

U2 Pin	Division	Frequency	Time Period
12	2	2.25 kHz	444 usec
11	4	1.125 kHz	888 usec
9	8	562.5 Hz	1.777 msec
6	16	281.25 Hz	3.555 msec
5	32	140.625 Hz	7.111 msec
4	64	70.312 Hz	14.222 msec
3	128	35.156 Hz	28.4 msec

These clock divisions are used to sequentially generate enable and disable relationships in the recording system.

C. Key (note) Switches and Multiplexing

Three divisions of the clock frequency are used for the timing functions in the recording process. Refer to Figure 1. Clock /2, /4 and /8 are connected to U 16, the assembly

multiplexer, for timing of the eight input bits. Clock /8 is inverted by U 7F and strobes or enables U 1. Clock /4 and Clock /8 are routed to U 6 Pin 1 and Pin 8 respectively to provide gating for the sustain pedal. Clock /16, /32, /64 and /128 are connected to the inputs of U 1 where they produce a sequential word enable gating. Thus, Word 0 (W 0) through Word 15 (W 15) are high outputs when not enabled and go to the low state for about 1.75 msec when enabled. The action produced is to enable one group of eight notes or bits (B 0 through B 7). Ten groups of eight notes are thus sequentially scanned for a total of eighty notes. See Figure 4 for Bit Assignments and Word Enabling. The low output provided to each group by U 1 enables any or all keys in that group, when depressed, to provide a low input into U 16, the assembly multiplexer. As can be seen in the schematic, Bit 0 through Bit 7 are directed into U 16. Resistors R 47 through R 54 pull up the inputs in to U 16. This pull up action insures that unless a definite low condition is observed at the inputs to U 16 the inputs will register a high condition which translates to a no-key depressed condition. Thus,

Input to U 16:
Low equals Note equals 0
High equals no Note equals 1

D. Pedal Switches

When W 0 goes low, it is conducted through current limiting resistor R 45 to Pin 1 of U 21 A, the non-inverting input. U 21 A is normally biased by R 46 so that Pin 5 is high which disables the common pin (at J 4 Pin 1) of the pedal switch. As will be remembered, a low is necessary to register a switch closure. Thus when W 0 occurs and takes this position low, Pin 1 of U 21 A goes low which also takes Pin 5 low which enables the pedal switches. Thus if the sustain pedal, for example, is depressed while W 0 occurs, a connection is made between J 4 Pin 1 and 2 through D 15, to Pin 14 of U 16 and is entered into the data assembly multiplexer. In an identical action, the soft pedal is entered into U 16 Pin 13.

E. Sync Word Generation

The sync word is generated in the following manner. U 21 C and D are biased through R 44 so that Pins 9 and 10 are normally high. When W 15 is selected and goes low, it is applied to Pin 12 and 13 of U 21 C and D through R 43 which current limits the enable signal. When this occurs, Pins 9 and 10 go low which provides a low to be passed through D 8, 9, 10, 11, 12, and 13 to Bit inputs 0, 1, 2, 3, 4, 5 and 7. Thus the sync word is entered in word 15 as six lows a

high and one low which occupies all the bits in that word. Note that a disqualified condition exists if a foreign object of a conductive nature (e.g., metal filings, pins, hair clips, paper clips, etc.) connects bit lines together. This causes the system to generate and record data frames with an invalid sync word. The system will not reproduce these passages.

F. Composition Multiplexer

U 16 is the assembly or composition multiplexer. See Figure 1 for its timing relationships. The clock signals applied on Pins 9, 10 and 11 sequentially enable the eight input lines so that data (high or low) may be registered. Simultaneously, each of the ten word enables are synchronously and sequentially selected. Thus, when W 0 is enabled bits 0 through 7 are selected and when the next word, W 1 is enabled bits 0 through 7 are again selected. This process continues until all sixteen words have been enabled and the process immediately repeats, producing a continuous sequence of data frames consisting of high and low levels corresponding to whether notes, pedals, and sync have been generated. At the output of U 16, Pin 3, we can observe this continuous data sequence. The output of U 16 is low for notes, pedals, or sync bits and high for no notes, etc. C 22 acts to reduce transients created by the switching action of U 16 and rounds off the leading edges of the data square waves. U 7 A functions as an invertor so that now for a note having occurred, a high level is produced and for no note having occurred, a low level is produced.

G. Frame Delay Registers

The output of U 7 A on Pin 2 is routed to three different points. First, it is directed to the key counter circuits in the bass and treble expression counters. Second, it is connected to Test Point 4 (TP-4). Thirdly, it is supplied to the input of the frame delay registers, U 12 and U 20. U 12 and U 20 provide one frame (128 bits) of delay by the following process. Data applied to U 12 Pin 1 is clocked, or allowed to change, through the 64 stages one bit at a time by the clock signal applied to Pin 2. U 20 provides a similar 64 stages of clocking action and the data provided at Pin 6 of U 20 is thus delayed precisely one frame or 128 bits and is in perfect synchronism with the rest of the system. This must be done so that the expression computation, which requires one frame, can be performed and the bits derived can be added to the data in the proper frame. Were this not done, any expression added to the data stream would occur the frame after the notes it was derived from which would degrade the realistic reproduction of the performance.

III. RECORDING SYSTEM (Cont)

H. Frame Double Generator Registers

U 25 and 29 perform an operation identical to U 12 and 20; however, the end result is different. Data from U 29 Pin 6 can be called the data double or data repeat because a note registered in one frame will always appear once more in the next frame through the action of the note doubler. This applies to the pedals and the sync word also. This doubling of notes and pedals provides smooth transitions and connections between notes in all musical passages. The two data streams are added in U 22 A which provides a high output when either of the inputs are high (refer to Figure 7 for OR gate truth table). Thus, when either Pin 8 or Pins 1 and 2 are high, Pin 9 is also high. U 5 B inverts the data and buffers it from the following stages.

I. Dynamic Expression Computation

Derivation of dyamics or expression from a purely electronic keyboard is relatively difficult and expensive. However, the PIANOCORDER system has been designed to accurately generate a dynamic expression level which faithfully corresponds to the slightest nuance and subtlest shading of expression of the artist. Generation of this intensity level allows the entire dynamic range of the performance to be accurately recorded and reproduced. Note that individual expression for the treble half and the bass half of the keyboard is independently created. Thus, a pianissimo in the bass section and a fortissimo in the treble section will be reproduced in precisely the manner in which it was created. The three sections of the computation system are the acoustic sensor, the key counter and the sustain pedal compensation circuitry.

1. Acoustic Sensor (Microphone).

The acoustic sensor is a good quality transducer element such as might be found in a microphone. Its dynamic element is sensitive to the pressure gradients of the sound waves generated by the piano transmitted to it through the atmosphere. It is mounted on the record board internally to the piano. It is acoustically isolated to an appreciable degree from external influence when the lower frame is installed. The sensor is mechanically isolated through the foam pad which connects it to the record board. It should be noted that striking the body of the piano during the recording process might induce a signal into the sensor which may generate a spurious level of expression. Normal operation of the keys and pedals will, however, in no way produce spurious conditions in the sensor's

performance. This sensor provides a means of transducing or converting the acoustic energy present in the form of sound pressure to an electrical voltage to which it corresponds (is analogous to). Thus, the greater the intensity of the performance, the greater the voltage produced at terminal E 1 on the record board. Capacitor C 1 couples this varying voltage while blocking any DC potential from the sensor. Resistor R 1 limits the current flow into amplifier U 15 C as well as determines the gain of the amplifier in conjunction with R 2. The AC or signal gain of U 15 C is approximately 100 as determined by the ratio of R 2 to R 1 (220 K/2K2 = 100). The output of U 15 C Pin 8 is divided into three paths. First, it returns through R 2 to the amplifier's input to act as the negative feedback path. This negative feedback increases stability of the amplifier as well as reducing distortion and determining gain. Secondly, it is conducted through R 5 into the bass intensity record level control R 6. Thirdly, it is conducted through R 8 to the treble record intensity control R 7. R 6 and 7 provide a convenient means of compensating for the acoustic output and balance of the piano to match it to the recording system's parameters. Increasing the output of R 6 or 7 generates more voltage which in turn creates more expression so that the system and the piano may be integrated into a system which truly reflects the touch of the pianist. The output of R 6 is again AC coupled and DC isolated through C 3. C 3 is a low impedance to all audio frequency signals and a high impedance to any DC voltage present. R 9 limits the current into U 15 B and determines the AC gain of the stage in conjunction with R 11 as was the case with the first amplifier stage U 15 C. Gain of U 15 B is approximately 20 but is decreased at higher frequencies by the lowered impedance of C 5 to high frequencies which feeds back more high frequency signal which decreases gain. The output of U 15 B at Pin 7 is developed across R 14 and again AC coupled, DC isolated, by C 7 which is also a low impedance to all audio signals present. The signal is now applied to a low pass, multiple feedback, active filter comprised of U 14 B, Resistors R 15, 16, 17 and Capacitors C 9 and 10. The filter is required to separate the bass signals present from the treble signals which are also present at the input of the filter. The output of the filter is on U 14 Pin 7 where only a varying DC level corresponding to the intensity of bass notes played. The treble information is processed in a similar manner with some deviations. The differences are that smaller coupling capacitors are used (C4 and C 8) which tends to reduce the amount of low frequency (bass) signal

passed because they increase in impedance as the frequency is decreased, thus performing some elimination of low frequency components. The treble signal is applied to a high pass multiple feedback, active filter consisting of U 14 C, and associated components. The action of this filter is conjugate to that of the bass filter so that the output of U 14 C Pin 8 consists of a varying DC level which accurately corresponds to the intensity of treble information present acoustically. Resistors R 3 and 4 form a voltage divider network which provides DC bias to the amplifiers to place them in their active operating regions. Capacitor C 2 acts to bypass ripple or noise at the bias point thus stabilizing the operation of the amplifiers. Resistors R 19 and 21 and Capacitor C 12 perform an identical function for U 14 B and C.

2. Key Counter

Since the operation of the key counter is identical for the bass and treble sections, only the action of the bass will be described. It should be remembered, however, that different words are enabling the action of the key counters so that expression is timed to coincide with the proper section of the keyboard. U 19 B and D form a bi-stable latch or reset-set (R-S) flip flop. See Figure 7 for symbol and truth table. This circuit has two stable output conditions which are either high or low (1 or 0). The set input is Pin 6 of U 19 B, the reset input, is Pin 13 of U 19 D. When Pin 6 goes low, the output of the flip-flop, Pin 4, goes to high. When Pin 13 goes low, Pin 4 returns to the low position. Pin 4 of U 19 B is thus high at the start of the bass keys (W 2) and low at the end of the bass keys (W 7). When U 19 B Pin 4 is high, the following gate, U 24 B, is enabled. The clock signal is applied to Pin 5 and key data to Pin 4. Thus, the output of U 24 B, Pin 6, is synchronized with the record system timing and counts only during the time the bass notes are enabled, words 2 through 7. This output is applied to U 28 Pin 2, the input of the 4 stage binary counter. Bits 2 and 4 are used which provide the following weighting: bit 2, 1 key; bit 4, 4 keys. Bit 2 (Pin 13) goes high when one key is down in the bass section. Pin 12 (bit 4) goes high when 4 keys are down in the bass section. Thus, both bits will go high when 5 bass keys are down. The output of U 28 is applied to the bass digital to analog conversion circuitry.

3. Digital to Analog Conversion

The bass digital to analog converter (DAC) consists of the following components: Resistors, R 28,

24, 29, 30, 31 and Diodes D 1, 2, 3. The digital to analog conversion is accomplished as follows. Resistors R 24 and 28 form a voltage divider network which divides the supply voltage to approximately +8 volts at TP 1, the bass threshold test point. When bits 2 and/or 4 from U 28 go high, the voltage across R 24 increases from its nominal bias point of +8 volts. The output of U 14 D, Pin 14 and Test Point 3 goes high to allow the following counter to count. When U 14 D Pin 14 is low, the following counter is disabled and does not count. U 14 D is biased so that the acoustic signal which was developed as previously discussed is present at U 14 D Pin 12. This point is biased by the voltage divider comprised of R 22 and 23 to approximately 6 volts DC. Thus, the acoustic voltage must also be present for U 14 D Pin 14 to go high. By this, it is meant that, for example, although 5 keys are depressed, test point 3 will remain low if there is no acoustic input to bias U 14 D on (output high). The situation would be produced if, for example, ten keys were very slowly depressed and held down, but no strings were struck and thus no sound was produced. Also note that the bass key counter bit 4 activates expression in the treble DAC. This feature is incorporated to compensate for the inherently louder bass half of the keyboard and to produce acoustic balance when loud passage are recorded in the bass section.

4. Sustain Pedal Compensation

The sustain pedal also activates the DAC in both the bass and treble section. This compensates for the increased intensity when the sustain pedal is used during recording. Note that this is no way affects whether or not the sustain or soft pedal are recorded. Again we use R S flip flops to set (enable) and reset (disable) the sustain pedal compensation. U 13 B and C comprise the flip flop used to activate sustain pedal compensation in the bass and U 13 A and D are used to compensate the treble DAC. The sustain pedal, when enabled by W 0 and recorded by depressing the pedal and closing the switch provides a low to Bit 1 and thus to U 6 B Pins 5 and 6. U 6 B acts as an inverter, thus, when the sustain pedal is on, and a low is provided to Pins 5 and 6, Pin 4 goes high and is thence transmitted to U 6 A Pin 2. When the CLK / 4 goes high on Pin 1, U 6 A Pin 3 can go low while at all other times, Pin 3 U 6 A will be high. U 7 C operates as an inverter. Thus, when U 6 A Pin 3 is low (sustain pedal on, CLK / 4 HIGH) Pin 7 U 7 C is low, Pin 6 is high. As in U 6 B, a HIGH for sustain pedal on is supplied to U 6 C Pin 9 and CLK / 8 must be high on U 6 C Pin 8 for Pin 10 to

go low. At all other times it will remain high. Also, as previously mentioned U 7 B inverts the low for sustain on at Pin 5 and presents a high for sustain pedal on at U 7 B Pin 4 (U 6 D Pin 12). Pin 11 of U 6 D is low when Pin 12 is high (sustain pedal on) and W 0 is HIGH on Pin 13. This low on U 6 D Pin 11 is inverted to U 7 D so that Pin 10 goes high when the above conditions have been fulfilled. A high at U 7 D Pin 10 sets the two R-S flip flops U 13 B and C and U 13 A and D so that their outputs on Pins 1 and 10 are high and thus increase the voltage across R 24 and R 27 which causes U 14 A and D Pins 1 and 14 to go high which causes the amount of expression to increase. Although notes may appear on bit B 1 and be enabled by CLK / 4, CLK / 8 no sustain pedal compensation can occur at the wrong time because U 6 D Pin 11 is gated off by W 0 on Pin 13. Note that sustain pedal compensation is reset at the end of every frame by W 15. When W 0 is low it is inverted through U 26 A and appears at U 6 D Pin 13 as a high which enables the flip flops to be set high only during W 0.

5. Composite Expression Counter

Expression has thus been translated to a high for loudness and low for not loudness at U 14 D Pin 14, dependent on the intensity and length of time sound is present. This intensity control signal is conducted to U 8 C Pin 13 where it acts as a gate for 2 X CLOCK to count expression levels into the bass composite expression counter, U 3. U 17 A acts as an overflow cut off circuit by keeping Pin 1 high for any count out of U 3 less than 31. When count 31 is reached, Pins 2, 3, 4 and 5 of U 17 A go high and Pin 1 goes low, a low on Pin 1 puts a low on Pin 11 of U 8 C which gates off or stops the clock counts going out of U 8 C Pin 10 into U 3 on Pin 1. U 3 operates in the following manner: when clock pulses are present on Pin 1, the five output lines go high to represent, in binary form, the count or stay low to represent no count. The five slots or bits represent 32 different combinations as represented in the figure below.

FIGURE 5
BINARY WEIGHTING DIAGRAM

Weight	Pin Number	Number										
		0	1	2	3	4	5	6	7	8...16		31
1	12	0	1	0	1	0	1	0	1	0	0	1
2	11	0	0	1	1	0	0	1	1	0	0	1
4	9	0	0	0	0	1	1	1	1	0	0	1
8	6	0	0	0	0	0	0	0	0	1	0	1
16	5	0	0	0	0	0	0	0	0	0	1	1

1 = high = true = greater than 10.5 VDC
0 = low = false = less than 1 VDC

When U 3 Pin 2 is high, counting proceeds normally, but when Pin 2 is briefly brought low (by W 0) the output Pins 3, 6, 9, 11, and 12 all go low and stay low until clock pulses are again gated into the counter and counting action occurs. This is termed the reset function and occurs every frame because W 0 occurs every frame. Thus, expression levels are constantly being developed which enables rapid dynamic changes in the performance to be precisely reproduced in the PIANOCORDER system. Therefore, at the output of U 3 we have in parallel form (five output lines) a binary number consisting of 5 bits or 32 unique numbers or levels which represent the intensity or expression of pianist.

6. Parallel to Serial Conversion.

The five parallel bits are converted to five bits in serial form (that is from individual highs or lows on five separate lines at the same time, to five bits in sequence through time on one line) by the operation of U 4 and its associated gates. U 4 is an 8 stage shift register with parallel-in serial-out operation which performs precisely the task its name implies. When W 14 is enabled or goes low, it is inverted by U 26 B and Pin 4 goes high. This high provides two actions. First, it enables U 4 to be loaded or accept the five bits presented to its inputs on Pins 4, 5, 6, 7, and 13. Secondly, it causes U 22 B Pin 6 to go high which causes U 8 B Pins 4 and 5 to go high, which allows the CLOCK signal present at Pin U 8 B Pin 3 to pass through the gate to Pin 6 and on to U 4 Pin 10. This allows the expression bits to be synchronously clocked into the shift register. Thus, W 14 enables (or more correctly called, loads) the shift register by taking the load pin high (Pin 9) and clocking the input bits into the shift register. When W 14 returns to

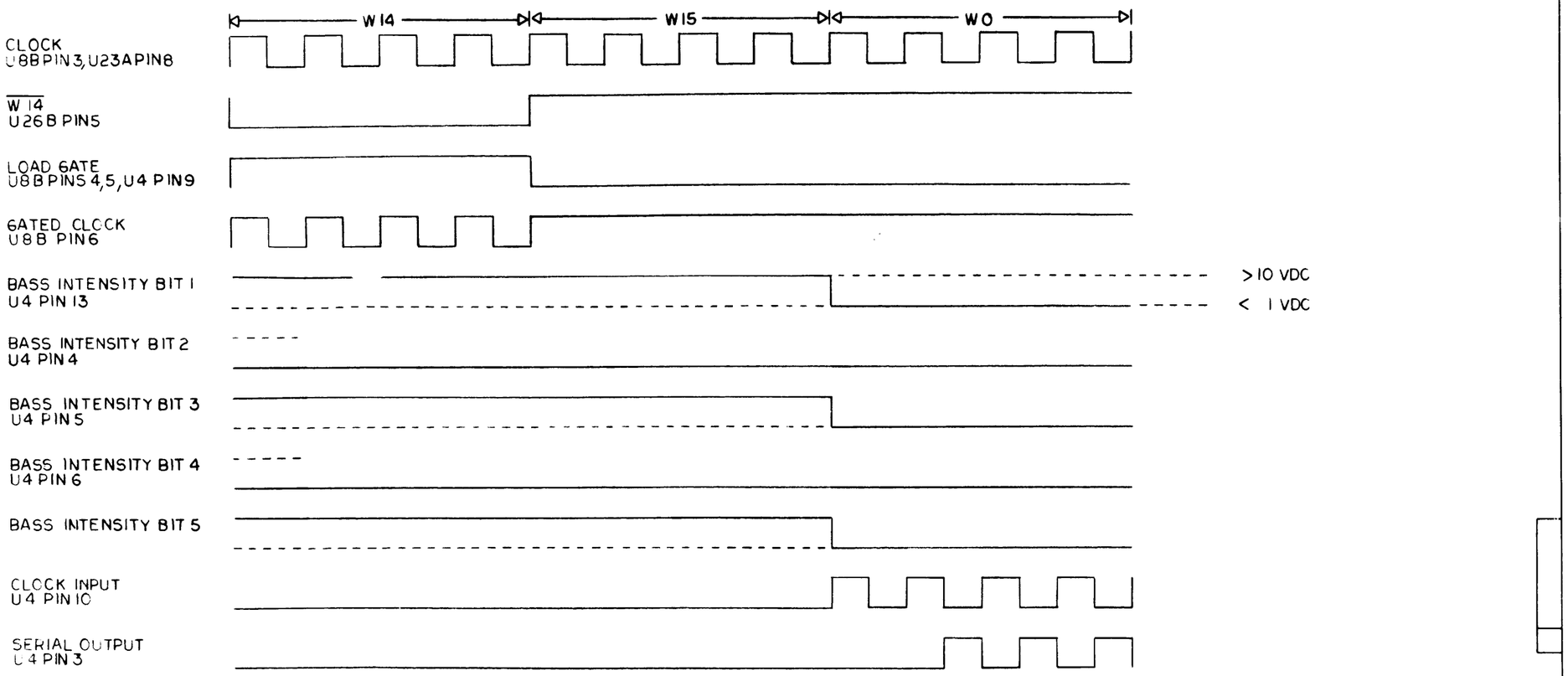
high, the shift register stores the five bits clocked into it but does not perform any other action. Now, when W 0 goes low, indicating the word in the frame for bass expression, several operations occur. W 0 is inverted by U 26 A so that Pin 2 goes high and causes U 22 B Pin 13 to go high which causes U 22 B Pin 6 to go high. NOTE: U 4 Pin 9 is NOT taken high by U 22 B. Taking U 22 B Pin 6 high takes U 8 B Pins 4 and 5 high also. This again allows the clock to pass through U 8 B from Pin 3 to Pin 6. Now, instead of transferring the 5 bits of information present on the inputs of U 4, into the shift register, the information present within U 4 is transferred out of the shift register in serial form on Pin 3. (See Figure 6 for timing relationships.) Inputs 1, 2, and 3 are hard wired low on U 4 so that these bits are always low. Inputs 1, 2 and 3 are loaded as zeros so that the pedal information in bits 0 and 1 may be preserved and word 0 thus consists of:

Bit 0	Soft Pedal	
Bit 1	Sust. Pedal	
Bit 2	Not Used	
Bit 3	Bass Intensity	Bit 1
Bit 4	Bass Intensity	Bit 2
Bit 5	Bass Intensity	Bit 3
Bit 6	Bass Intensity	Bit 4
Bit 7	Bass Intensity	Bit 5

Once the bits have been serially clocked out of the register, it is cleared and waiting to be loaded by W 14 and the cycle is repeated. Bass expression bits are gated into the data frame through U 5 A. When W 0 goes high on Pin 2, bass expression bits are passed from Pin 1 to Pin 3 and inserted into the proper frame and proper bits within that word. Treble expression bits are generated in an identical manner through its respective circuitry. Notice however that different words are used to gate the expression circuitry.

REVISIONS				
SYM.	DESCRIPTION	BY/MN	DATE	APPR'D.

FIGURE 6
PARALLEL TO SERIAL TIMING DIAGRAM



ITEM	PART NO.	DESCRIPTION
REQ'D. PER ASSY.		LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
1. BREAK ALL SHARP CORNERS .015 MAX.
2. SURFACE ROUGHNESS 63 MICROINCH R. M. S. MAX.
3. DIAMETERS TO BE CONCENTRIC WITHIN .003 T. I. R.
4. FILLET RADIUS .010 MAX.
5. THREADS — CLASS 2

MATERIAL

FINISH

TOLERANCES UNLESS OTHERWISE NOTED
ANGLES ±0° 30' FRACTIONS ±1/32 DECIMALS .XX ± .030 .XXX ± .010

DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

DRAWN BY Marilyn Morgan DATE 4/79

CHECKED

APPROVED

PROJ. ENG.

SUPERSCOPE. CHATSWORTH, CALIFORNIA

DWG. TITLE
PARALLEL TO SERIAL TIMING DIAGRAM

RELATED DWGS.

DWG. NO.

REV.

SCALE

SHEET OF

DASH NO. | NEXT ASSY. | MODEL NO.

APPLICATION

55-MAR 0168

III. RECORDING SYSTEM (Cont)

J. Data Frame Composition.

At TP 7 we can observe the completed data frames consisting of: bass expression, bass notes, treble expression, treble notes, pedals, and sync word. The data frames present at TP 7 are now supplied to the bi-phase converter.

K. Bi-phase Converter.

The Bi-phase converter consists of U 11 and U 19 A. The purpose of this circuitry is to convert the high and low conditions present at TP 7 into one of two frequencies. An input of a 0 or low (representing that no note or pedal has been sensed) is converted to half the clock frequency which is 2.25 kHz (444 usec period). A 1 or high is converted to the clock frequency of 4.5 kHz (222 usec period). This operation is accomplished in the following way: data frames are received at U 19 A Pin 2. Bi-phase data frames are supplied at the output on U 11 B Pin 15. U 11 A operates as a divide by 2 circuit which, as described before, divides the 2 X CLOCK frequency down to the clock frequency (supplied to the rest of the timing circuits as previously described). The clock frequency is supplied to U 19 A Pin 1. When U 19 A Pin 2 is low (0) Pin 3 remains HIGH, this high takes Pin 10 and 11 of U 11 B high and the output of Pin 15 is one half of twice the clock input, or the CLOCK frequency. When U 19 Pin 2 is HIGH, the clock is passed from U 19 A Pin 1 to Pin 3 which alternately takes Pins 10 and 11 of U 11 B high and low at the clock rate. Thus, the output (Pin 15) will change every other time 2 X CLOCK (Pin 13) goes from high to low, thus generating the bi-phase code used for recording.

L. Power Up Delay Circuit.

The output of the bi-phase converter is next applied to the power up time delay cut off circuit consisting of U 5 C and D and R 55, D 17 and D 18. This circuit prevents data frames now in bi-phase format from being supplied to the tape recorder until all record circuitry has had time to come up to full power supply potential and stabilize itself. This insures that only valid data will be passed to the tape recorder and recorded. The action of the circuit is as follows: When +12 volts is first applied (Record button down) C 18 passes the initial charging current and slowly charges from ground potential to approximately 11 volts DC. Until the positive side of C 18 reaches about 7 VDC Pin 9 of U 5 C remains low so that U 5 C is effectively gated off, that is, any data present at U 5 C Pin 8 is blocked from passing to Pin 10. The time required for C 18 to charge up to the voltage necessary to gate data through U 5 C is determined by the values of R 55 and C 18. The time re-

quired with the values shown is about 300 msec. U 5 C also inverts the data. U 5 D is connected as an inverter which corrects the polarity inversion caused by U 5 C as well as providing drive current to Q 1.

M. Output to Tape Recorder.

Q 1 acts as a common emitter buffer amplifier and driver for the bi-phase signals. A positive or high on its base (B) will cause it to saturate which will develop about 10.5 VDC across R 56. When a negative or low is presented to the base it cuts off the transistor and no voltage is developed across R 56 because Q 1 is cut off and allows no current to pass through it. The amplitude and wave shape of the bi-phase signal is not altered through the action of Q 1 but the available drive current is greatly increased. The output of Q 1 is routed to J 3 Pin 3 and thence conducted to the tape recorder.

N. Tape Recorder Equalization Circuit.

Bi-phase data is received on Pin 10 of J 002 (Pin 3 J 101) and is developed by R 107. C 108 isolates any DC potential from the recording head but passes the bi-phase signal to the head drive equalization circuit consisting of R 115 and C 109. H 001 performs the dual function of recording or writing data as well as reproducing or reading data. The equalization circuit provides matching the bi-phase signals to the record head by limiting the drive current and passing the leading and falling edges of the square wave bi-phase signal.

O. Tape, Record Head, Signal Interrelationship.

Detailed explanation of the interaction of the record head, tape and drive signal is beyond the scope of this description. Briefly, the signal present at the record head causes flux radiations emitted from the record head gap to be retained on the tape in the form of flux reversals in a sequential manner as the tape is transported past the recording head. H 001 is a ½ track (mono) cassette head with a resistance of about 150 ohms and an impedance at 1 kHz of about 600 ohms.

P. Functions of the Tape Recorder in Record Position.

When the PT 100 PIANOCORDER digital cassette tape recorder is placed in the record mode by depressing the red record button on top of the recorder, several actions occur simultaneously. S 101 is the record-playback switch and is shown in the playback position. We will now examine each section of this switch to determine its function. S 101-1

switches control of the speed of the motor from variable (in the playback mode) to a predetermined value (as determined by R 128 in record mode). In the record position, R 128 can be calibrated to provide recordings that are precisely (within .5%) on speed. Note that the velocity at which the tape is traveling when recording is critical to the range with which it can be reproduced. That is, if R 128 is miscalibrated, a recording can be made and reproduced but the range of the tempo (tape velocity) will not be as great as possible before loss of synchronism is incurred. This is a factory adjustment and should never be attempted by the field technician. Also note that the velocity of the tape when varied by the tempo control during reproduction in no way affects the pitch or frequency of the reproduced passages. The pitch of the performance is determined by the frequency of oscillation of the strings as determined by the temperament of the individual instrument. S 101-2 provides a triple function. In the position shown (playback) +12 VDC is provided to Q 101-1, 2 and Q 102-1, 2 which amplify the signal reproduced in the playback head. In the record position S 101-2 provides + 12 VDC to S 002, the Pause Switch, which is normally on or closed (when pause button is not depressed or down). Thus, 12 VDC is supplied to J 101-2 and output to the record board ONLY if the recorder is in the record position and the pause button is not depressed. S 101-2 also provides + 12 VDC through R 125 to H002, the erase head. H 002 saturates its magnetic field thus polarizing or magnetizing the tape and erasing any flux reversals or stray fields imprinted upon the tape. This action assures that the tape will not contain any false flux reversals once the record head has imprinted its signals, since no flux reversals will remain on the tape past the erase head in the record position. Thus, note that it is possible to erase previously recorded performances if they are not of the type or quality desired. However, it is also possible to erase material that is desired to be kept if the operator operates the record button. S 101-3 connects the record-playback head to the appropriate circuitry. In the position shown, H 001 acts as the playback transducer. In the record mode (switch opposite that shown) the head records or writes the signal information on the tape as described previously. S 101-4 transfers the output of Q 102-2 to the input of the playback board in the position shown (playback). In the opposite position, it terminates the input to the playback board through R 113 to ground. The other function accomplished when the record button is depressed is the closing of S 1001 which provides DC power to the servo-motor to activate the tape transport mechanism.

Q. Power Supply and Decoupling.

All power for the recording system is operated from the +12 VDC power supply and is routed through the tape recorder

in the record mode and supplied to the record board. Thus C 101 stablizes the supply voltage and reduces any ripple or noise present on the supply lines. On the record board C 19 and 20 perform identical functions. CMOS logic and bipolar linear circuitry is used in the record section and the actions of C 19 and 20 are entirely adequate to reduce ripple, noise and transients on the +12 supply lines to a level that provides reliable operation of the recording system. The +12 also lights the power lamp, Q 001, on the front of the tape recorder to indicate +12 VDC is present. R 101 limits the current through Q 001 to a safe value.

IV. PLAYBACK SYSTEM

A. Description.

The playback system consists of the tape recorder, the playback logic board, the three driver boards, the power supply and the note and pedal solenoids. As its name implies the system decodes and reproduces the information on the cassette tape into a faithful musical performance of whatever is recorded. To accomplish this task, several sophisticated data generation and distribution systems are employed.

B. The Tape Recorder.

The tape recorder, as previously described, recovers the bi-phase signals recorded or stored as magnetic flux reversals on the cassette tape. When S 101 is in the playback position (shown in the schematic diagram), H 001 is connected as a playback head. The flux reversals recorded on tape radiate lines of flux which induce a voltage in the playback head proportional to the amplitude and polarity of the flux on the tape. A wave form that is approximately 5-7 mv p-p is present between J 114 and J 115 (common). This signal is routed through S 101-3 and coupled through C 107 to the input of Q 101, Pin 2. R 126 terminates the playback head and reduces gain of Q 101-1. The outputs of Q 101 and Q 102, Pins 1 and 7, are biased to approximately ½ supply voltage by R 131. Thus, with no signal applied, R 131 should be adjusted so that the outputs of Q 101 and 102 are at approximately +6 VDC. C 101 acts as a stabilizer on the +12 VDC line bypassing ripple or current surges to ground. In a similar manner, C 102 stabilizes the bias supply line to Q 101 and 102 bypassing any ripple or voltage changes to ground. The AC gain of Q 101-1 is determined by the ratio of R 108/ R 126 which is approximately 13. C 103 decreases the gain as frequency increases thus eliminating spurious high frequency noise and stabilizing the amplifier at high frequencies insuring that it does not oscillate. C 104 ac couples the output of Q 101-1 to the input of Q 102-1 and blocks any dc component. R 109 performs two functions. First, it limits the current into Pin 2 of Q 102-1. Secondly it determines the AC gain of Q 102-1 in conjunction with R 110. Thus, the ratio of R 109/R 110 sets the gain of Q 102-1 to approximately 41. C 105 acts as did C 103 in the first stage to stabilize the amplifier with respect to high frequency instability. Signals observed at Q 102-1 Pin 1 will be approximately 2.7 V p-p for 0's or 2.25 kHz and slightly less for 1's or 4.5 kHz. The signals at this point resemble distorted sine waves. When the tempo knob is increased to maximum, the 0's may slightly flatten on the top and bottom of the waveform indicating saturation as been reached. As in the first two stages, C 106 couples the AC signal and R 112/R 111 set the AC gain at about 41.

The gain of Q 102-2 insures that all signals at the output are square waves with clean leading and falling edges. R 114 limits output current of Q 102-2. R 113 terminates the output of the tape recorder in the record mode. Data out of the recorder is supplied from J 002 Pin 12 to the playback board.

Speed of the transport is controlled by several control potentiometers. The only one which is user controllable is R 104, the front panel tempo control. R 129 sets the speed of the motor when R 104 is set in its center, detented, position. An external tempo controller, when plugged into J 004, replaces R 104 with an external control which may be used to remotely control the speed or tempo of the reproduced performance. Additional circuitry in the tape recorder is used later in the reproduction process and will be described in its appropriate section.

C. Playback Board +12 VDC Section

The +12 VDC section of the playback board is optically isolated from the +5 VDC section so that should a fault occur in the +12 section no shock hazard could occur through operation of the tape recorder.

The +12 VDC section consists of Q 1, Q2, R1, 2, 3, 8, 26 and the light emitting diode half of U 11 (Pins 1 and 2). Data is received from the tape recorder at Pins 12 and 8 of J 2 and is applied through current limiting resistor R 1 to the base of Q 2. R 3 and R 8 act as a voltage dividing network to bias Q 2's emitter to approximately 5 VDC. Thus, the input signal must be at least +6 VDC before Q 2 will conduct. This action eliminates the possibility of noise or line transients generating data in the playback system. R 2 acts as a load for Q 2 to develop the signal to drive the base of Q 1. Q 1 amplifies the input signal and provides sufficient current to properly operate the light emitting diode half of the optical coupler. When Q 1 is turned on it saturates and provides a low impedance path from +12 VDC return through R 26 the current limiting resistor, through the LED and Q 1 and on to the +12 VDC supply line. The light emitting diode radiates brightly when it is saturated, but does not emit light when Q 1 is cut off. Therefore, the electrical signal is optically coupled through the beam of light while no electrical connection is made. Thus, the two power supply systems are entirely isolated. The 47K resistor, from the collector of Q 1 to the base of Q 2 provides positive feedback to insure snap action thus improving transition times and insuring a measure of stability by positively biasing the transistors into either the saturating or cutoff states. This is the only circuitry derived from the +12 supply, from here on all logic circuitry is powered by the +5 VDC supply.

IV. PLAYBACK SYSTEM (Cont)

D. Playback Board, +5 VDC Section.

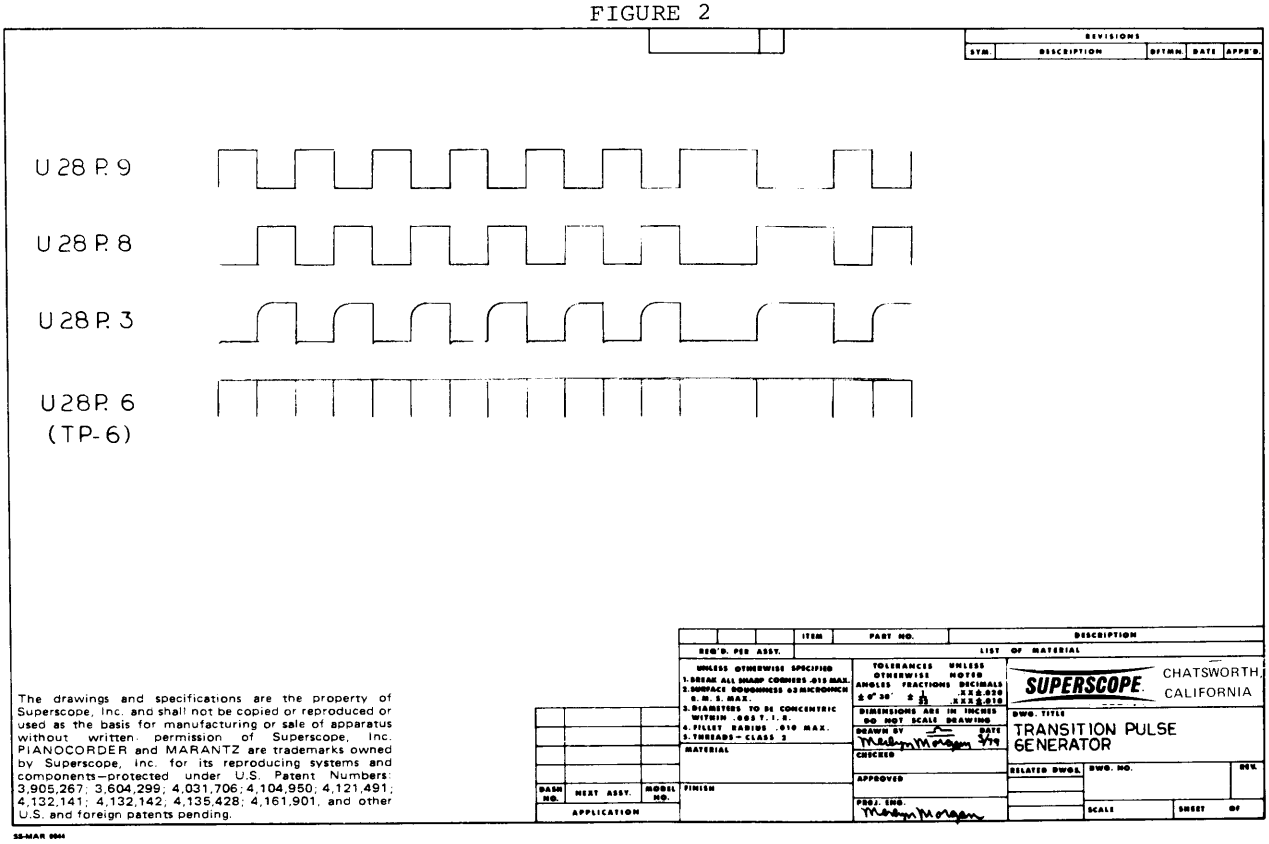
1. Input Circuit and Transition Pulse Generator.

Pins 4 (Emitter or E), 5 (Collector or C), 6 (Base or B) of U 11 represent a photon detecting transistor. This transistor acts in the following manner:

Photons of light impinging on the base-emitter junction forward bias the transistor allowing current to pass from the emitter to the collector. Thus, when input signals are causing the light emitting diode in U 11 to emit light, it causes the photon detector transistor to conduct (saturate). R 6 develops or biases the photon emission relative to the base. R 7 develops the output voltage of the photon detector and supplies the signal to the input of U 14 Pin 11. U 14 is an inverting schmitt trigger. This unit has the properties of not changing state until a predetermined level has been reached, thus eliminating noise signals below a certain threshold.

U 28 and C 1 form a transition pulse generator. The action of this circuit produces negative trigger spikes of approximately .5 usecs duration in response to transitions, either from high to low or low to high. See Figure 2 for the relative timing and waveforms present.

FIGURE 2



IV. PLAYBACK SYSTEM (Cont)

Also refer to the logic diagrams and truth tables, Figure 7. The operation of this circuit is as follows: when a low is present at U 28 Pin 9 a high will be present at U 28 Pins 1, 5, 8. The inverse is also true; thus, a high at U 28 Pin 9 will result in a low at Pins 1, 5, and 8. Thus, when U 28 Pin 8 changes from low to high, Pin 3 also goes from low to high, but is delayed slightly by the charge time required of C 1 to allow the full potential to be realized. When Pin 3 (and 12) finally goes high Pins 11 and 4 are taken low and since Pin 5 is still high a negative pulse is produced, whose duration is determined by the value of C 1. This negative pulse is called EDGE and is connected to the input of the CLOCK generator, U 27, and to the input of the data generator U 14 Pin 9. It is easily accessible on TP-6.

2. Recovered Clock Generation (Data Pulse Generator).

The recovered clock is generated by U 27 which is a "one shot" multivibrator and associated circuitry. When the negative trigger pulse is applied to Pin 5, the output Pin 6 goes low and U 27 begins to time out. The time out is governed by the rate that C 2 charges through R 9 and R 10. D 3 provides a low resistance discharge path for C 2. The charge time is set by R 9 to be 3/4 of a bit which generates a waveform depicted in Figure 3 (U 27 Pin 6). Once U 27 has timed out, Pin 6 returns high and is ready to be reset. Thus at U 27 Pin 6 we have reconstructed a periodic waveform of known duration which can be used to synchronize or clock the decoding of the data in a repeatable, reliable manner which synchronizes with incoming data frames. U 19 B acts as a DC amplifier which expands the range in which U 27 can properly decode the data into a reliable clock signal. Thus, a range of ±15% from the nominal center is achieved. This action is achieved by varying the DC level at the junction of R 10 and C 2, thus changing the charge time of R 9, C 2. R 16, 17 and C 16 form a low pass filter which produces a DC voltage at PIN 6 the inverting input to U 19 B. The non-inverting input, Pin 5 is connected to R 19. R 18, 19, 73 form a voltage divider network which is used as the reference input for U 19 B. R 19 is the 3/4 bit range adjust. It is adjusted so that a clock signal can be properly generated through the entire tempo range. This is verified by the fact that the fine tuning lamp remains extinguished throughout the entire tempo range. R 92 provides degenerative feedback. R 20 limits the output current to the junction of C 2, R 10. In addition to producing a clock signal (D pulse) at Pin 6, U 27 also produces the D PULSE or CLOCK or

complement at Pin 1. This signal is used for various timing functions which will be described later.

3. Data Generator.

U 2 and U 14 D are the data generator. By comparing the CLOCK signals at Pin 2 and the edge of Pin 3, decoded data is produced at Pin 5. Thus U 2 converts bi-phase edges into lows or zeros for no notes and highs for notes at this point. See Figure 3. This data is supplied to Pins 1 and 2 of U 7, an 8 stage serial-in parallel-out shift register which has two functions. First, it provides a one bit delay of the data from U 2. It also provides a means of recognizing the sync word. This function will be fully described later. Thus, U 7 provides the decoded data now in simple binary form to the following places: J 4 Pin 3, J 5 Pin 8, J 6 Pin 3, U 23 Pin 13 and U 12 Pin 13.

4. Sync Detector.

a. Sync Bits and Word Detector.

The sync detector consists of the following components: U 7, U 8, U 16, U 4A, B, D, E, F; U 3C, D; U 5, U 9, U 1 A, U 14 B, C and U 15 C and D. The sync detector identifies the sync word generated in the record board (refer to record circuit description for generation) which consists of six highs or ones, a low or 0, and another high or one. Thus, the sync signals consist of one word eight bits long. When the sync signal is not present, as when no data is present, the detector causes U 5 Pin 11 to go high, causing U 14 Pin 6 to go low, which causes U 15 Pin 6 to go low. This low causes two actions. First, it lights the fine tuning lamp on top of the tape recorder, indicating loss of sync. Secondly, it clears (or resets to zero) all latches in the driver boards which store whether notes are to be sounded or not. It also clears or releases the pedal sole noids. Thus, no notes are played and all registers are cleared and held ready to accept new data. As will be shown, valid data frames with good sync word must be generated twice before this register clearing function can be disabled. Following is a description of how this is accomplished.

Word 15, which contains bits 121 through 128 (counts 120 through 127), provides the means of

maintaining synchronism between the playback system and the data provided from the cassette tape. The data frames are clocked into shift register U 7 (serial-in, parallel-out, see Figure 3) on Pins 1 and 2. The CLOCK signal is applied on Pin 8. The sync word is in its proper position when:

TABLE 3
SYNCWORD SHIFT REGISTER CORRESPONDENCE

Location	Bit	Logic Level
U 7 Pin 13	Bit 120	1 (HIGH)
12	121	1 (HIGH)
11	122	1 (HIGH)
10	123	1 (HIGH)
6	124	1 (HIGH)
5	125	1 (HIGH)
4	126	0 (LOW)
3	127	1 (HIGH)

As will be recalled in the description of the record board, Bit 126 (bit 6 of the sync word) is a 0. This bit is inverted by U 14 B. The output of U 7 is applied to the inputs of U 8, a 10 input NAND gate. As with any NAND gate, the output remains high unless all input pins are high (in this case ONLY when a proper sync word is present). Thus, when the sync word occurs, and only when the sync word occurs, U 8 Pin 8 goes LOW.

Bit 6 of the sync word (Bit 126 of the frame) is inverted so that sync cannot be detected if data frames of all ones are present.

b. Counter Bit Detector.

To prevent generation of a valid sync gate at any time other than bit 128 (count 127), U 16 gates the output count from U 21 and U 22. Thus, when count 127 occurs, CTR Bits 1, 2, 4, 8, 16, 32 and 64, which are on the input pins to U 16, are all high causing the output, Pin 8, to go LOW. See Figure 3. The operation of U 21 and U 22 are described in the section covering system synchronization.

c. Sync Counter.

When power is initially applied and no valid data frames are being processed, U 9 A and B are

cleared when U 26 Pin 8 goes low. This sets Pins 9 and 12 of U 9 low and Pins 8 and 13 high. This keeps U 1 A Pin 6 high because Pin 2 remains low. In this condition U 21 and 22 can be at any random count. Now assume that the playback board starts processing a valid data frame, for example at bit 60, and clock signals are generated by U 27 at Pin 6. The first clock pulse causes U 26 to trigger and set its output, Pin 8, high. Now U 1 A is initialized. U 1 A Pins 4 and 5 are high as the flip flops have not processed two valid data frames. Pin 1 of U 1 A now toggles high and low with the applied clock pulses and, since all other pins are now high, this toggling is passed to the output, Pin 6, which causes U 21, 22 to load a count of 127 into their outputs which causes U 16 Pins 1, 2, 3, 4, 5, 6, 11 and 12 to simultaneously go high and drive Pin 8 low. This action repeats until the sync word is decoded through the actions of U 7 and U 8 (refer to section D.4.a.). Thus, at this time, U 8 Pin 8 goes low and initializes the sync counter. When U 8 Pin 8 and U 16 Pin 8 go low indicating count 127 (end of frame) and sync word, U 4 A Pin 2 and U 4 B Pin 4 go high. Now U 3 C Pin 8 goes low driving U 4 D Pin 8 high. This is applied to U 9 B Pin 7 which causes the output, Pin 9, to go high when the clock pulse on Pin 5 goes high. This also takes U 9 B Pin 8 low. Now, two conditions can occur. Either another valid frame can be processed or an invalid frame can be processed. Let's consider the circuit operation where an invalid frame is processed.

A faulty data frame is detected in two ways. Either the sync word is not correct or not present, or the frame does not contain the proper number of bits (128). First, let's assume the sync word is defective. As described, one valid data frame has been processed. U 21, 22 count clock pulses and when count 127 (Bit 128) is reached U 16 Pin 8 goes low, but since there is a defective sync word U 8 Pin 8 does not go low. U 4 A Pin 2 goes high and U 3 D Pin 1 goes low because Pins 12 and 13 are high. U 4 E Pin 10 thus goes high. U 3 C Pin 8 stays high because Pin 9 has stayed low (no sync word detected). Now, since U 9 A Pin 13 must be high and U 5 C Pin 10 is high, Pin 8 goes low. Thus, U 5 A Pin 1 is low, which gates Pin 3 high even though Pin 2 is high. U 5 A Pin 3 high sets U 9 B Pin 9 low and Pin 8 high when the clock goes high, thus eliminating the register of one valid data frame. The system is thus reset to its quiescent state.

Now, let's assume that the sync word is good but the frame does not contain 128 bits. Now, when the sync word is detected, U 16 Pin[8] does not go low because 128 bits have not been counted. Thus, U 3 D Pin 12 goes low but Pin 11 remains high because Pin 13 is low. Therefore the sequence is repeated and U 5 A Pin 3 is high, thus resetting U 9 B Pin 9 low and Pin 8 high.

Next let's assume the second and following data frames are all valid. As described, the first valid data frame has set U 9 B Pin 9 (and U 5 B Pin 4) high and Pin 8 low. When the next sync word is detected U 5 B Pin 6 goes low driving U 4 F Pin 12 high setting U 9 A Pin 12 high and Pin 13 low when the clock pulse goes high. Thus U 5 D Pins 12 and 13 are both high and 11 is low.

Once two valid data frames have been registered, the following action occurs when further valid frames are received. U 3 D Pin 11 remains high because Pin 12 is low when Pin 13 is high. Thus U 4 E Pin 10 holds U 9 A Pin 3 low insuring that Pin 13 is also high. This holds U 5 A Pin 3 low and Pin 2 is held high because U 3 D Pin 11 is also high. Therefore U 5 A Pin 3 is low which insures U 9 B Pin 9 is high and Pin 8 is low. This drives U 14 C Pin 6 high and U 15 C Pin 6 high. When this occurs, the fine tuning lamp is turned off. Refer to tape recorder schematic for connection of the fine tuning lamp. The register clear function is supplied to the tape recorder on J 101 Pin 12. Following through Q 002, the azimuth, fine tuning or sync LED and R 120, the current limiting resistor, we come to the + 5VDC line. Thus when J 101 Pin 12 is high, Q 002 is placed between two high potentials and does not light. When this point goes low (when sync is lost) Q 002 is between a low and high potential and lights, informing the operator of the condition of the reproduction system. This high also enables all latches in the driver cards to receive data. Also note U 5 D Pin 11 is connected to U 25 Pins 8 and 12 which enable the pedal logic.

5. Missing Pulse Detector and Register Clear

U 26 is connected as a retriggerable one shot multivibrator in a configuration similar to U 27. This circuit is set to time out or switch Pin 8 to low if the triggers supplied to its input Pins 3 and 4 are not retriggered within a specified time. Thus, it causes

Pin 8 to go low if there is a missing pulse or no clock pulse generated by U 27 at Pin 6. This low at U 26 Pin 8 causes several actions to occur. First, it takes Pins 2 and 6 of U 9 A and B low which sets the outputs, Pins 9 and 12 to low. It also causes U 1 A Pin 6 to go. Clearing U 9 A and B sets Pins 12 and 9 low. As soon as valid data pulses are received and clock signals are generated, U 26 Pin 8 goes high and the inputs to U 1 A, Pins 1, 2, 4, 5 are all high and Pin 6 goes low, thus initializing U 21, 22 to start counting from Bit 0. The BLANK signal also clears U 7 by taking Pin 9 low and clears U 2 by taking Pin 1 low.

6. System Synchronization and Data Distribution.

When the sync counter has been set to indicate two frames of valid data have been processed, the system is ready to distribute data in the following manner. The CLOCK applied to U 22 Pin 14 and U 21 Pin 14 causes them to count in the up direction. The up-down line is hard wired for counting up only. The enable line of U 22 Pin 4, is tied low to enable it to count up. U 21 is enabled by the ripple clock output of U 22 Pin 13. Thus, when U 22 has reached its maximum count it enables U 21 to start counting thus preventing spurious counting pulses from activating U 21. Refer to Figure 3 for detailed timing sequences. Thus, we can see how CTR bits 1 - 64 are sequentially generated (or in other words, these bits go high). CTR Bits 1, 2, and 4 are used as the 1 of 8 address lines to the driver cards and the expression latches. These determine which place a bit is to be stored in its word of eight bits. CTR Bits 8, 16, 32, and 64 cause U 20 to generate a one of 16 word enable pulse which is the complement of the word enable signal generated in the record board. Refer to the description of the record board and the record timing sequence as well as the playback timing sequence for complete description. The outputs of U 20 go low sequentially as enabled by the counters U 21 and U 22.

For example, when U 20 Pin 3 goes low (W 0) the first word of the frame is enabled. This is the word which contains the pedal and bass expression information. While this remains low, CTR bits 1, 2, and 4 are counted by U 21 and 22 generating 8 bits or slots. These eight slots are synchronized with data from U 2 by the CLOCK and are thus supplied to the expression latches. In a similar manner, bass notes are sequentially decoded word by word and supplied to the driver boards to be sounded as a note or not sounded depending on what is recorded on the tape. Treble notes are

decoded in an identical manner by the appropriate word enable.

The clock signal applied to U 3 A Pins 1 and 2 is inverted at Pin 3. The R-C time delay network of R 15, C 4 causes the input of U 3 B to change state later than the input to U 3 A. The CLOCK pulse is again inverted through U 3 B to maintain proper polarity and is supplied to U 3 B Pin 6 as the delayed CLOCK signal. This signal is applied to the strobe input of U 20, thus causing a slight (about 1.5 usec) delay in enabling the outputs. This is done to "deglitch" the system and allow the outputs of U 20, 21, 22 to settle to stable states. The delayed clock signal also strobes the word enable output so that once the data transfer is accomplished, the enable line returns to high (not enabled). This prevents noise, crosstalk, glitches or other spurious signals from producing false information. Further, this delayed clock signal is inverted by U 14 F and applied as the clock input to the sync counter flip flops. This is done for the same reason as the counters, namely, to allow the system to settle into its stable state so that no switching transients (spikes) are mistakenly read as valid data.

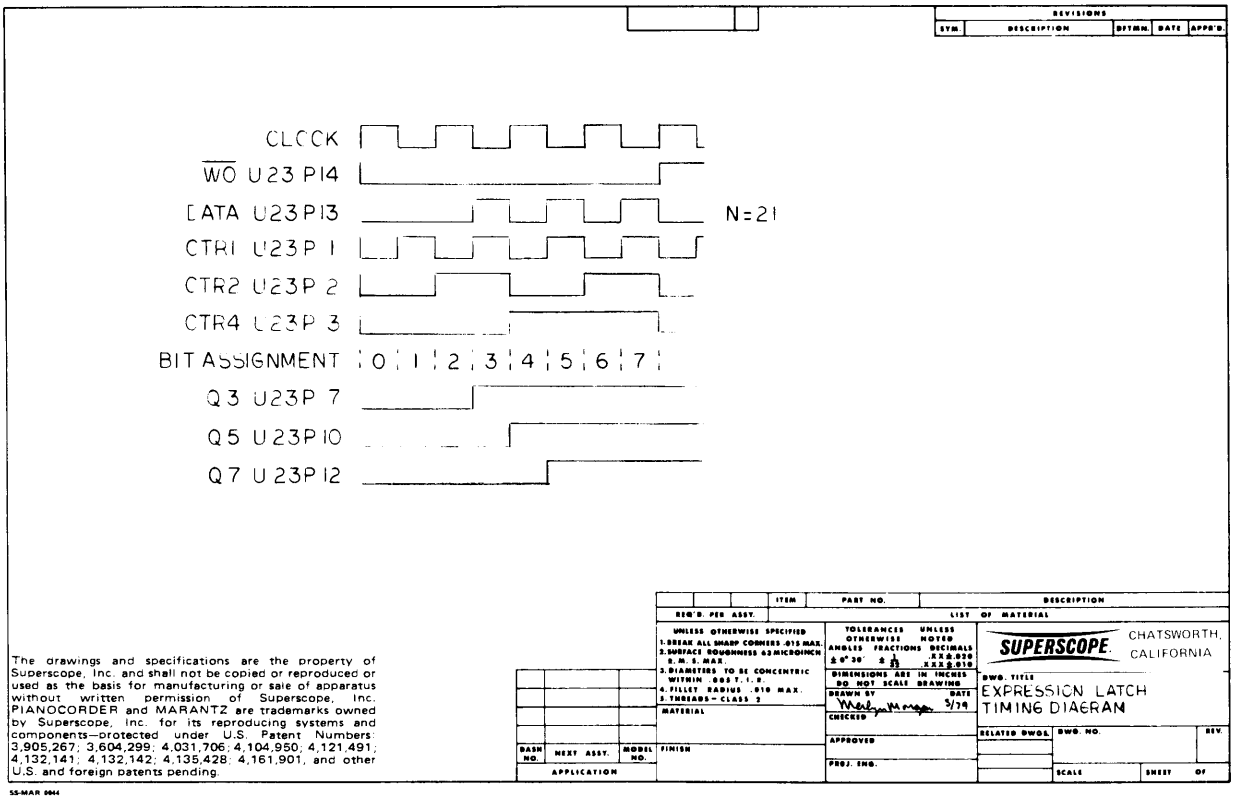
IV. PLAYBACK SYSTEM (Cont)

7. Expression Decoding

a. 8 Bit Latches

The bass expression and soft and sustain pedal information is decoded and stored in U 23, the treble and control bits in U 12. When U 20 Pin 1 goes low it enables U 23 to accept data (refer to Figures 3 and 8 for timing) on Pin 13.

FIGURE 8



The place in the 8 bits where it is stored is determined by the state of the address lines A 0, A 1, A 2 which are determined by the state of CTR Bits 1, 2, 4.

TABLE 5
TRUTH TABLE FOR CTR 1, 2, 4

BIT	1	2	3	4	5	6	7	8
CTR 1 = A 0	0	1	0	1	0	1	0	1
CTR 2 = A 1	0	0	1	1	0	0	1	1
CTR 4 = A 2	0	0	0	0	1	1	1	1

In an identical manner the treble latch, U 12, decodes and stores the control bits and the treble expression bits. The function of the control bits is described in detail later.

The output of the expression latch stores the expression bits throughout the frame because even though A 0, A 1 and A 2 are constantly being addressed (since U 22 is always counting clock pulses) the latches don't accept or write the data present on Pin 13 because Pin 14 is high thus disabling the write function of the latch and insuring it remains in the read mode for the duration of the frame.

b. Digital to Analog Converter (DAC).

The bass digital to analog converter consists of U 17 C, U 24, R 21, 22, 23, 24, 25 and 46. The treble converter consists of U 17 B, U 13, R 27, 28, 29, 30, 31 and 50. U 13, 17 and 24 are quad bi-lateral switches. When their control Pins (5, 6, 12, 13) go high the switch closes allowing any positive voltage level analog signal to pass from the input to the output (for example from Pin 10 to Pin 11). For example, if expression bits 1, 3 and 5 are on (expression level = 20) U 17 C, U 24 A and B pass the DC bias present to their outputs. This DC bias produces a corresponding DC voltage across R 46 which is proportional (analogous) to the intensity level and the bias level present. Thus, a binary (digital) expression level is converted to an analogous dc voltage level. Note the different values of resistors used in the output of the converter. These values contour or weight the various binary (digital) values to produce a logarithmic curve for reproduction of the expression. This is done so that the dynamic

range of the expression precisely corresponds to a human being's transducer and bio-computer. In other words, it matches how people hear different intensities of sound. Conversion in the treble section is identical.

c. Pianissimo, Fortissimo and Biasing of Digital to Analog Converter.

As was stated above, the DC bias potential is supplied by U 18 Pin 7 to the inputs of the converter switches. Refer to tape recorder schematic for derivation of control voltage sources. In the tape recorder +5 VDC is supplied on J 101 Pin 10 and returned on Pin 6. R 116, 117 and variable resistors R 118, R 119 form a variable voltage divider network. At J 101 Pin 8 a variable voltage from 0 - 3.8 VDC is available for fortissimo biasing. A J 101 Pin 9 0 - 1.8 VDC is available for pianissimo biasing. These bias values are user variable. They are derived from the pianissimo and fortissimo controls on the front of the cassette recorder and the value of the output of the digital to analog converter feedback (through R 36 in the bass section). The fortissimo control provides a control voltage of 0 - 3.8 VDC to R 57, 61. C 12, 11 bypass noise on the control lines to ground eliminating spurious expression levels while the pianissimo and fortissimo controls are being rotated. R 57, 58 form a voltage divider which scales down the fortissimo voltage to a range of 0 - 1.9 VDC. In a similar manner, the pianissimo control supplies 0 - 1.8 VDC to the junction of R 59 and 36. Thus, when the pianissimo control is turned to maximum, U 18 B is biased on and Pin 17 provides a DC voltage output which is gated through the switches to produce a composite DC Voltage across R 46. A portion of the voltage is fed back through R 36 to the inverting or - input of U 18 B. Now assume that the fortissimo control is set to the mid position. The individual bits are gated on or off according to which bits are high (on) or low in the data frame being processed. Now assume that maximum expression is recorded on tape, that is, bits 1 through 5 are all high or on. This gates all switches in U 24 and U 17 C on. Now, since the fortissimo control is turned half way down, the DC level present at U 18 Pin 7 is half the level present when at maximum, thus, only half the bias level is present at the output. Thus, the maximum loudness level present is set by the fortissimo control to half maximum value.

The minimum level is set by the pianissimo control. This control is similar in action to the fortissimo control but it sets the minimum level or DC bias to which the output of U 18 can descend. The minimum intensity controls R 37, 68 set the point at which the power delivered to the solenoids is enough to just sound all notes when the hammers strike the strings. With the pianissimo and fortissimo controls adjusted to their minimum position (CCW) the alignment tape is played and the minimum intensity controls rotated until all notes stop playing, then slowly rotated until all notes play at their absolute softest pianissimo. U 18 C and D act as buffer amplifiers between the varying DC voltage present at their inputs (pins 10, 12) and its outputs. Gain of the amplifier is determined by the ratio of R 39/R38 which is about ten. At TP 2 and TP 3 we can thus measure the operation of the latches DAC and buffer amplifier to determine if this section of the expression decoding is operating properly.

d. Note Expression Ramp Generator.

The note expression ramp generator is comprised of Q 4, 5, U 19 A, C, D, R 51, 52, 53, 54, 55, 56, 77, C 9, and C 10. The output of this circuit is at U 19 Pin 1 and is a sawtooth wave of approximately 2.4 V p-p amplitude. The operation of the circuit is as follows. Resistors R 53, 56 form a voltage divider network which biases U 19 C and D into their active regions. R 51, 77 bias Q 5 into conduction. Assume Q 4 is initially cut off, that is, the collector-emitter (C-E) junction is high resistance, this causes Q 5 to allow C 9 to charge from ground, through collector to emitter of Q 5 through R 52 to the + 5 VDC line. Charging time is set by the values of C 9 and R 52. When C 9 reaches a certain voltage it causes the output of U 19 D to change state from low to high. This transition is delayed (and integrated) by R 53, C 10 to produce a narrow pulse at the output of U 19 C Pin 8. This narrow pulse causes Q 4 to turn on and saturate, which causes the C-E junction to be low resistance which allows C 9 to discharge through this low impedance. U 19 A is connected as a non inverting unity gain buffer amplifier. It isolates the ramp generator circuit from being loaded down by the following stage, the pulse width modulators. Thus, at TP 1 we observe a ramp with a time period of approximately 5 msec (200 Hz) and an amplitude of about 2.4 V p-p.

e. Pedal Ramp Generator

The pedal ramp generator consists of U 6 B, U 10 D, R 76, 101, 83, 84, 85, 86, 79, 80, 81, C 17, 18. R 76, 83, 10 form a voltage divider which biases U 6 and 10 into their active regions. C 17 bypasses ripple and noise on the bias line to ground. U 6 is used as a voltage comparator with gain set by the ratio of R 86/R 84 which is less than unity. R 85 is the pull up or collector load resistor for U 6. R 79 isolates the output of U 6 from the input of U 10 as well as limits the drive current available. U 10 operates as an integrator. C 18 is the feedback element. R 80 provides feedback from the output to the input of the comparator. R 81 is the pull down resistor for U 10 D. At TP 5 is a 20 kHz triangle or ramp waveform (time period of 50 usec) which is used as the carrier frequency for the pulse width modulators which operate the pedals.

f. Pedal Logic and Control.

Pedal logic is obtained through the following action. U 25 gates both soft and sustain pedals. When the presence of the sustain pedal is decoded through the action of U 23 Pin 5, U 25 Pins 5 and 6 also go high causing Pins 4 and 19 to go low. Thus, Pin 10 goes high. Note that should sync be lost and the register clear go high, this will turn off both pedals. When U 25 C Pin 10 goes high the following actions occur. C 15 charges through R 94, D 8, R 82 and R 100. C 15 acts as a low impedance source during the low to high transition, placing a high potential on R 94. The rate of charge of C 15 and thus the amount of power used to pull in the sustain pedal solenoid and is controlled through variation of R 82. Once C 15 has fully charged, it rapidly discharges through D 6, the voltage necessary to hold the solenoid in being developed by the voltage divider composed of R 94, 74, 75, and 100. The soft pedal logic pull in and hold circuitry is identical, with one exception which is decribed in the following section.

g. External Soft Pedal Control.

Refer to the tape recorder schematic. The soft pedal switch on the front of the cassette recorder provides a means of applying the soft pedal at any time desired (except during system

non synchronization). The soft pedal switch is connected to ground when off and connected through R 121 to + 5 VDC when on. This action causes the chains of events to occur precisely as described with the sustain pedal.

h. Pulse Width Modulators and Output Drivers.

Expression or the force that varies the intensity with which the solenoids operate the keys is developed in the pulse width modulators U 10 B and C. The action of U 10 C is described, U 10 B acts in an identical manner.

The 200 Hz ramp is applied through R 41 to the non inverting or + input of U 10 C. The ratio of R 42/R 41 sets the gain of the ramp signal in the modulator (approximately 150) so that above a certain threshold the input ramp will saturate the comparator. Varying DC voltage which represents the intensity of the performance is the control signal. Refer to Figure 9.

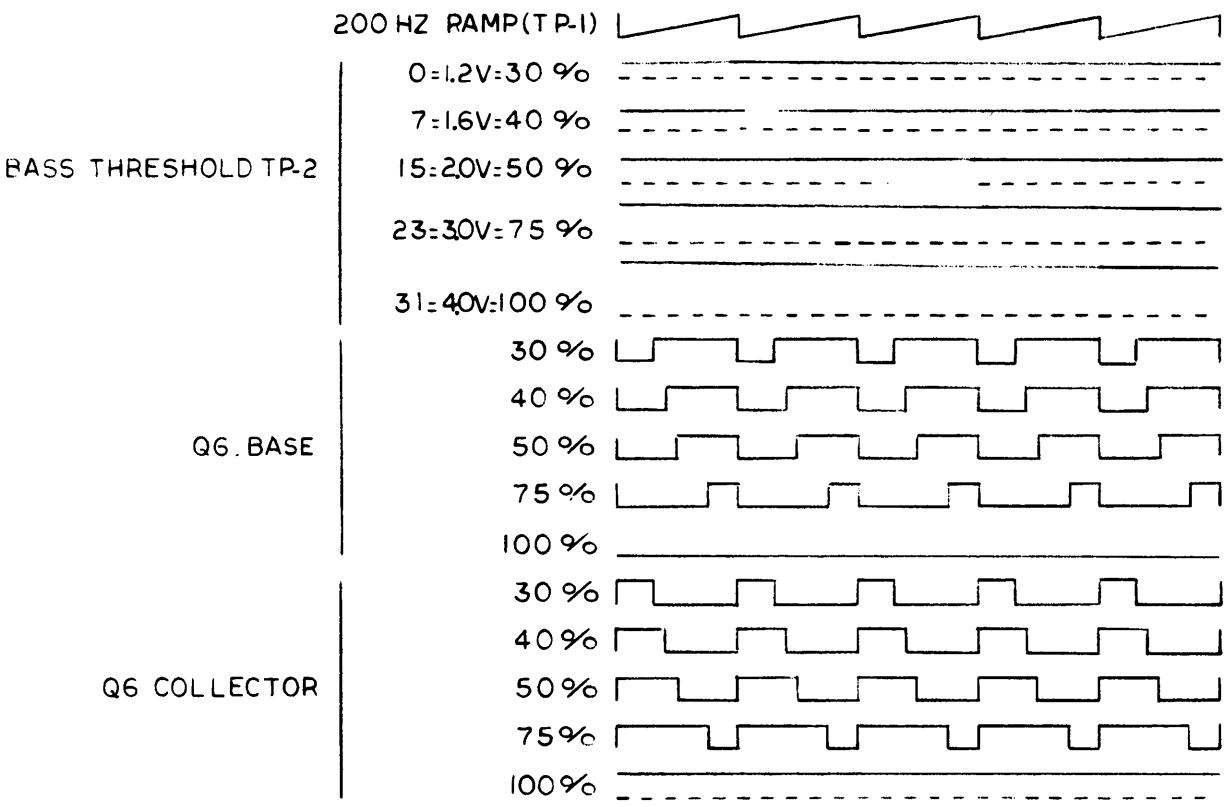


FIGURE 9.

REVISIONS				
SYM.	DESCRIPTION	DFTMN.	DATE	APPR'D.

ITEM	PART NO.	DESCRIPTION
REQ'D. PER ASSY.	LIST OF MATERIAL	

UNLESS OTHERWISE SPECIFIED
1. BREAK ALL SHARP CORNERS .015 MAX.
2. SURFACE ROUGHNESS 63 MICROINCH R. M. S. MAX.
3. DIAMETERS TO BE CONCENTRIC WITHIN .005 T. I. R.
4. FILLET RADIUS .010 MAX.
5. THREADS – CLASS 2

MATERIAL

FINISH

DASH NO.	NEXT ASSY.	MODEL NO.
APPLICATION		

TOLERANCES UNLESS OTHERWISE NOTED
ANGLES ± 0° 30' FRACTIONS ± 1/32 DECIMALS .XX ±.020 .XXX ±.010

DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

DRAWN BY Merlyn Morgan DATE 3/79

CHECKED

APPROVED

PROJ. ENG.

SUPERSCOPE. CHATSWORTH, CALIFORNIA

DWG. TITLE
PULSE WIDTH
TIMING DIAGRAM

RELATED DWGS. | DWG. NO. | REV.

SCALE | SHEET OF

SS-MAR 0044

1. Notes.

From Figure 9 the following operation can be determined. The control input (from the digital to analog converters) changes the point at which the comparator U 10 C switches from off to on. Thus, as the expression level is lower, the bias level is lower and the point at which the modulator changes state from off to on is sooner. The minimum expression level causes the modulator and thus expression data to be on for only approximately 35% of the ramp duration or about 1.75 msec. As the expression increases, the modulator is biased later and later into conduction. Thus, as the expression level increases, the time that the output of the modulator is off increases (U10C P8). At full expression the modulator is cut off and not biased into conduction at all. This signal is then inverted by Q 6 so that the signal at J 6 Pin 13 is high for 30% to 100% of the time depending on the amount of expression. R 43 acts as a current limiter. Thus, as a high or positive is applied to the base (B) of Q 6 the collector goes low and inversely, as the base goes low the collector (C) goes high. R 44 serves to develop this drive voltage. The expression drive is thus a pulse wave form varying in duration. The length of time the pulse is present provides the appropriate power to the solenoid which causes the piano action and thus the hammer to strike the string with the exact intensity encoded in the data frame. Treble expression is formed in an identical manner.

2. Pedals.

The pedal pulse width modulator operates in a similar manner. However, only two widths pulse are used. The first width, the initial or "pull in" width, is controlled by R 72, 82. These resistors provide virtually 100% modulation. The bias voltage is reduced to approximtely 30-40% modulation in 1 second as C 4 discharges through D 4 and the bias voltage is derived from the resistive voltage divider network consisting of R 4, 5, 93. D 7 prevents the discharge of C 14 from affecting the dc voltage level at the junc-

tion of R 5, R 93 which would affect the amount of modulation during "hold in". The capacitors from U 6 Pins 4, 7 to ground reduce noise when both pedals are on.

i. Expression Cutoff Circuit.

As in the record board, a circuit is provided to delay outputting any expression until all the power supply circuitry has had enough time to charge all components to full potential. This circuit is comprised of U 6 D, R 91, 90, 95, 96, 97 C 23, D 9 and 10. This circuit operates as follows: When power is initially applied, R 95 pulls the bases of Q 3 and 6 high through isolating diodes D 9 and 10. U 6 Pin 10 is biased by the voltage divider R 90, 96 to about 1.5 VDC. U 6 D Pin 11 is initially biased higher by C 23 which initially passes the turn off edge of power up and is slowly charging from ground through D 11 and R 90 to its maximum value. When this value is reached (in approximately 7 msec) U 6 D changes state and Pin 13 now goes low and D 9 and 10 are reverse biased, which allows normal expression to be passed through Q 3 and 6. R 197 acts as a feedback path to provide snap action when U 6 changes state.

j. Control Bits.

U 12 decodes two control bits as well as treble expression. These two control bits are supplied to the center driver board only. Their action will be described in the explanation of that board.

k. Power Supply Decoupling.

Capacitors C 5, 6, 7, 8, 19, 20, 21, 22 decouple current spikes on the + 5 VDC line. The type of logic family used in the playback board, TTL, draws considerable current when changing state and these capacitors are strategically placed throughout the playback board to minimize variations on the + 5 VDC line.

E. Driver Boards.

1. End Drivers

We can now examine the inputs and outputs of the driver boards to determine how data is transferred from

the playback board to the individual note solenoids. Only the bass end driver board will be described as the treble driver board is identical in operation except for the word enables provided. Word enables W 1, W 2, W 3 and W 4 are supplied on Pins 13, 9, 8, and 12 respectively of the bass driver board. When these enables go low the associated 8 bit latch (U 1, 2, 3, or 4) is enabled and can accept or write data. Addressing is supplied on lines A 0, A 1, and A 2. The operation is the same as that described in the expression latches (see Figure 8). See Figure 11 for note latch timing.

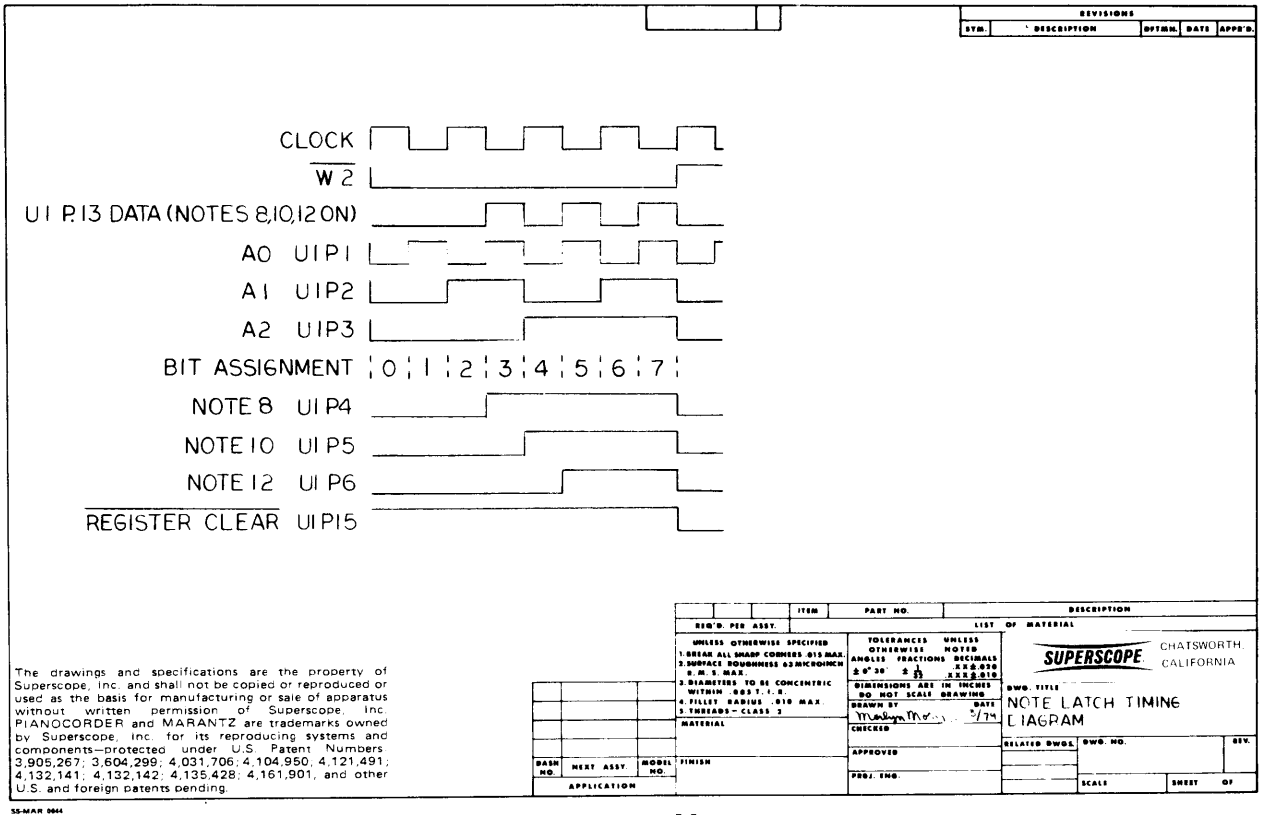


FIGURE 11

From Figure 11 it is clear how the word enables allow notes to be transferred into the latch on Pin 13 while A 0, A 1, A 2 gate in sequence the eight latches so that they hold any data (notes) in their outputs. As explained previously, although data is always present at Pin 13 and the latch is constantly addressed by A 0, A 1, A 2 no data is transferred into the latch until the enable line, W 0, goes low. Thus, in sequence W 0 through W 9 on all three driver boards are enabled when brought low from U 20 on the playback board. As previously explained when U 1 Pin 15 is high, data is written or stored. When Pin 15 goes low, the latch performs two functions. First, they stop accepting any new data. Secondly, they clear all existing notes in outputs Q 0 through Q 7 so that no solenoids are on. Expression is developed to each note in the following process. We will use U 5 as our example as all other notes are gated in a similar manner. Individual notes are output from U 1 on Pins 4, 5, 6, 7, 9, 10, 11 and 12 corresponding to bits 0 through 7. The line goes high when a note is present. Now, assume bit 0 (U 1 Pin 4) goes high indicating that the note is to be struck. The high is applied to U 5 Pin 5. Applied to U 5 Pin 4 is the expression gating signal. Recalling that the expression signal is a pulse wave form, which is variable in duration, it can be seen that if Pin 5 is high then the output of U 5 B, Pin 6, will also be high only as long as Pin 4 is also high. Thus, if Pin 4 is high for only 30% of its cycle, the note will sound with minimum intensity because the note solenoid will be receiving drive power for only 30% of the total note time and no energy for the remaining 70% of the cycle. For full intensity (fortissimo) the cycle is 100% and the note is sounded with maximum intensity. NOTE: Full dc supply (180 VDC) voltage is always applied to the note solenoids which allows them to operate in a linear manner. The high at U 5 B Pin 6 representing a note is supplied through D 34 to the base (B) of Q 1. D 34 steers the current from U 5 B to the base of Q 1 preventing reverse current flow and also isolating the + 5 VDC section from the + 170 VDC section should a failure occur in either section. R 1 develops the output of U 5 B so that when U 5 B Pin 6 is high the collector emitter junction of Q 1 is saturated (has a low resistance). This allows current to flow from the + 170 VDC return line, through Q 1 to the individual note solenoid and to +170 VDC. The function of D 1 is to reduce the current or voltage spike (or transient) produced by the collapsing electromagnetic field of the individual solenoid when it is turned off. Operation of all note solenoids is identical. C 2 and C 3 reduce noise and transients present on the + 5 VDC

supply lines to U 1, 2, 3 and 4. D 17 prevents polarity reversals on the 170 VDC line. C 1 reduces ripple, noise and transients on the 170 VDC line. R 33 limits the current flowing from the + 170 VDC return line to the + 5 VDC return line to prevent damage to +5 VDC components in case of an open circuit in the +180 VDC return circuit.

2. Center Driver.

The center driver board operates notes with expression in a manner identical to the end driver boards. Additional control bits 1 and 2 perform one additional function.

TABLE 6
TRUTH TABLE FOR CONTROL BITS 1, 2

CONTROL BIT 1	CONTROL BIT 2	FUNCTION
0	0	Note 44 gets bass expression; notes 45 and 46 get treble expression
1	0	Notes 44, 45 and 46 get treble expression
0	1	Notes 44, 45 and 46 get bass expression
1	1	Not Used

If control bit B 1 is high and Bit B 2 is low, U 8 Pins 5, 6, and 8 are high, thus U 8 pin 10 must be low regardless of Pin 9, and Pins 3 and 4 must also be low. Thus U 8 A Pin 1 inverts data from Pin 2 which is the treble expression line. In a similar manner when Bit 2 is low, U 7 Pins 5, 6, and 9 are low, U 7 Pin 4 is high, Pin 1 must be low. U 7 C inverts treble expression from Pin 8 to 10 then is inverted from Pin 11 to 13 thus maintaining polarity and passing treble expression to U 5 B. In a similar process it can be seen that were the polarities of bit 1 and 2 reversed, bass expression would be passed to U 4 C and U 5 B. These bits have been encoded in the Superscope Tape Laboratories to faithfully represent performances derived from Ampico and Welte reproducing piano rolls.

3. Pedal Drivers.

The driver circuits for the pedal solenoids are mounted on the power supply. The driver for the pedal

solenoids leaves the playback board at J 3 Pins 5 and 7. Refer to the Power Supply Schematic for further description. The soft pedal signal is received at J 1 Pin 3 on the power supply. Sustain pedal signal is on J 1 Pin 1. Since the operation of both circuits is identical, only the soft pedal circuit will be described. The 20 kHz square wave is applied to the base (B) of Q 5 and appears unchanged on the emitter. Q 5 is an emitter follower used to increase the current of the pedal signal to drive the light emitting diode (D 17) and the following stage. When Q 5 is brought into conduction by a positive signal on its base and a conduction path is formed from + 5 and + 170 VDC return lines through D 17 causing it to illuminate. Further, the path flows through R 20 which limits current in the path and through the E-C junction of Q 5 to + 5 VDC. The output of Q 5 is conducted through R 14, which limits the available drive current and D 13 which is a current steering diode isolating the +5 from the + 170 VDC sections in case of failure. Drive signal is developed across R 15 to turn Q 7 on. Q 7 is a common collector amplifier. When the base (B) goes positive the transistor conducts completing the path from + 170 VDC return through the emitter-collector junction, and out to the soft pedal solenoid on J 3 Pin 1. The current flows through the soft pedal solenoid and returns to the power supply at J 3 Pin 2. FS 3, a 1 amp fast blow fuse, opens if the pedal solenoid draws excessive current. D 14 is in parallel with the pedal solenoid and reduces electromagnetic interference generated when the solenoid turns off and the collapsing magnetic field generates it characteristic inductive transients. The diode connected between the junction of R 14, D 13 and the collector of Q 7 prevents transients of reverse polarity affecting the operation of Q 7.

V. TEST EQUIPMENT REQUIRED FOR SERVICING

The following equipment is recommended for servicing the PIANOCORDER Reproducing System:

1. DP-100 MAINTENANCE KIT

2. 10 A 0-140 VAC VARIAC

3. GOOD QUALITY MULTIMETER, DIGITAL OR ANALOG DISPLAY, BUT SHOULD BE PORTABLE (BATTERY OPERATED)

4. DUAL TRACE OSCILLOSCOPE WITH TRIGGERED SWEEP. NOTE: IF THE SCOPE HAS A THREE WIRE OUTLET (GROUNDED), A THREE WIRE TO TWO WIRE ADAPTOR MUST BE USED TO LIFT THE GROUND OF THE SCOPE. USING A GROUNDED SCOPE CAN INSTANTLY DESTROY THE PIANOCORDER SYSTEM. REFER TO THE SECTION ON GROUNDING FOR MORE INFORMATION.

VI. ALIGNMENT PROCEDURE

The alignment procedures are described in depth in the installation and field service manual. Refer to the particular section for detailed instructions.

VII. TECHNICAL SPECIFICATIONS

Refer to section 7 of the owner's manual for the technical specifications.

POWER SUPPLY ASSEMBLY

(Part Number 100-01F0-411 or refurbished, 100-01F0-41W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-02D142-1	BRACKET	
2	1	100-11A008-1	POWER TRANSFORMER	
3	1	100-04D016-1	PC BOARD ASS'Y	
4	1	3110CB162T200	CAPACITOR	MEPCO/ELECTRA OR EQUIV
5	1	3110HB123U015	CAPACITOR	MEPCO/ELECTRA OR EQUIV
6	1	CC3	MOUNTING BRACKET	NATIONAL CAP
7	1	CA2	MOUNTING BRACKET	NATIONAL CAP
8	7	TDF11-7-5ST	OVAL HEAD RIVET AL. .156/.150 DIA x 15/64 LG	NATIONAL RIVET
9	1	100-02B156-1	FUSE LABEL	
10				
11	4	TDF11-9-ST	OVAL HD RIVET AL. .156/.150 DIA x 9/32 LG	NATIONAL RIVET
12	2	#6-32UNG-2A	PAN HD, STEEL, 5/8 LG	PHILLIPS
13	2	#6-32UNG	NUT - SQ. STEEL	
14	2	#6	LOCKWASHER	

P.W. BOARD ASSEMBLY POWER SUPPLY

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05D016-1	P.W. BOARD	
2	A/R	SOLDER		
3	8	1A119-10 OR EQUIV.	FUSECLIP UL LISTED	
4	1	ABC 12 AMP	FUSE, UL LISTED	FS1
5	1	LITTLE FUSE 313-01.5	FUSE	FS2
6	1	100-11A006-1	DIODE BRIDGE 6A	D1
7	8	IN4004	DIODE	D1,2,3,4,6,7,13+16
8	4	MR752 OR P600D	DIODE	D8 THRU D11
9	4	IN4935	DIODE	D14, D15, D19, D20
10	2	LITRONIX RL-4850	LED	D17, D18
11	1	LM723	I.C. VOLTAGE REGULATOR	U1
12	1	MC7812CT	I.C. VOLTAGE REGULATOR	U2
13	1	2N2222, T018	TRANSISTOR	Q1
14	1	TIP-41	TRANSISTOR	Q2
15	2	100-02A159-1	TRANSISTOR	Q5, Q6
16	2	MJE13004	TRANSISTOR	Q7, Q8
17	1	100-11A012-1	TRANSIENT SUPRESSOR	RV1 K201J7
18	1	100-11A015-1	THERMISTOR	RT1
19	10	100-10B004-1	PIN .045 SQ	
20		DELETED		
21	1	350209-1	CONN, 2 PIN HEADER	J2 (AMP)
22	1	350429-1	CONN, 3 PIN HEADER	J6 (AMP)
23	1	350430-1	CONN, 4 PIN HEADER	J5 (AMP)
24		DELETED		
25	1		RESISTOR, 0.22, 3W, 10%	R1
26	2	312-001-1A	FUSE UL LISTED	FS3, FS4
27		DELETED		
28	3		RESISTOR, 220, 1/4W, 5%	R4, R15, R16
29		DELETED		
30	2		RESISTOR, 1.5K, 1/4W, 5%	R6, R9
31	1		RESISTOR, 2K, 1/4W, 5%	R7
32	1	PIHER PT15ZB470 RED	POTENTIOMETER 470	R8
33		DELETED		
34	1		RESISTOR, 8K, 7W, 10%	R12
35		DELETED		
36	2		RESISTOR, 10, 1/2W, 5%	R14, R17
37		DELETED		
38		DELETED		

P.W. BOARD ASSEMBLY POWER SUPPLY

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
39	1		RESISTOR, 330, 1/4W, 5%	R19
40	2		RESISTOR, 47, 1/4W, 5%	R20, R21
41	1	NICHICON CORP. 25 ULA - 2200	CAPACITOR, 2200uf, 25V	C1
OR	1	MATSUSHITA ECE - T25R222SU	CAPACITOR, 2200uf, 25V	C1
42	4	MATSUSHITA ECE - A25V220L	CAPACITOR, 220uf, 25V	C2, C4, C5, C6
43	2	CERAMIC AXIAL	CAPACITOR, 0.01uf, 50V	C7, C9
44		DELETED		
45	1	100-02D103-1	P.W. BD. MTG. BRACKET	
46	4	60-11-5791-1674	INSULATOR, SILICONE TIP-32	CHOMERICS
47	4	#4, 5/16" MIN O.D.	WASHER, FLAT	
48	4	2671	WASHER, FLAT, NYLON	H.H. SMITH
49		DELETED		
50	4	#4-40 x 3/8 LG	SCREW, PHILLIPS	
51	4	TDF-11-9-ST	RIVET, OVAL HD, AL 5/16 DIA x 9/32	NATIONAL RIVET
52	4	#4	WASHER, LOCK, SPLIT RING	
53	4	SWS-411	WASHER, NYLON SHOULDER	MICRO PLASTICS
54	4	#4-40	NUT	
55	1	7717-43	PAD, TRANSISTOR	THERMALLOY

P.W. BOARD ASSEMBLY, 16 KEY SWITCH
(Part Number 100-04D0-061 or refurbished, 100-04D0-06W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05D006-1	P.W. BOARD	
2	1	100-02C124-1	GUIDE, SWITCH	
3	16	100-02B157-1	SWITCH	S1 THRU S16
4	16	1N914 OR EQUIV.	DIODE	D1 THRU D16
5	2	09-66-1091 OR EQUIV.	HEADER	J1, J2
6	1	22-16-2161 OR EQUIV	CONNECTOR	J3
7	A/R		SOLDER	
8	5	TAAX12-11-ST	RIVET, OVAL HD, ALUM, .065/.062 DIA X 11/32 LG	NATIONAL RIVET
9	16	T0-40-09	WASH-AWAY SPACER	

P.W. BOARD ASSEMBLY, 32 KEY SWITCH
(Part Number 100-04F0-051 or refurbished, 100-04F0-05W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05F005-1	PW BOARD	
2	1	100-02D126-1	GUIDE, SWITCH	
3	32	100-02B157-1	SWITCH	
4	32	IN914 OR EQUIV	DIODE	D1-D32
5	1	1-640099-6 OR EQUIV	HEADER	P1
6	1	22-16-2161 OR EQUIV	CONNECTOR	J1
7	A/R		SOLDER	
8	9	7AAX2-11-ST	.065/.066 DIA X 11/32 LG. RIVET OVAL HD ALUM	NATIONAL RIVET
9	32	TO-40-09	WASH-AWAY SPACER	

EXPRESSION BOARD ASSEMBLY
(Part Number 100-04D0-101 or refurbished, 100-04D0-10W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05D010-1	P.W. BOARD	
2	1	4515B	INTEGRATED CIRCUIT	U1
3	3	4024B	INTEGRATED CIRCUIT	U2, U3, U9
4	1	4051B	INTEGRATED CIRCUIT	U16
5	1	4027B	INTEGRATED CIRCUIT	U11
6	4	4031B	INTEGRATED CIRCUIT	U12, U20, U25, U29
7	2	4014B	INTEGRATED CIRCUIT	U4, U10
8	2	4161B	INTEGRATED CIRCUIT	U27, U28
9	3	4073B	INTEGRATED CIRCUIT	U8, U23, U24
10	1	4075B	INTEGRATED CIRCUIT	U22
11	2	4049B	INTEGRATED CIRCUIT	U7, U26
12	1	4043B	INTEGRATED CIRCUIT	U13
13	4	4011B	INTEGRATED CIRCUIT	U5, U6, U18, U19
14	2	LM324	INTEGRATED CIRCUIT	U14, U15
15	1	3401	INTEGRATED CIRCUIT	U21
16	17	1N914	DIODE	D1 THRU D17
17	1	2N5172	TRANSISTOR	Q1
18	2		RESISTOR, 1.0m, 1/4W, 5%	R39, R40
19	1		RESISTOR, 510K, 1/4W, 5%	R20
20	1		RESISTOR, 390K, 1/4W, 5%	R37
21	1		RESISTOR, 220K, 1/4W, 5%	R2
22	6		RESISTOR, 100K, 1/4W, 5%	R11, R12, R22, R23, R25, R26
23	4		RESISTOR, 15K, 1/4W, 5%	R15, R29, R32, R33
24	1		RESISTOR, 82K, 1/4W, 5%	R42
25	13		RESISTOR, 10K, 1/4W, 5%	R3, R4, R13, R14, R19 R21, R24, R27, R30, R35, R41, R43, R45
26	2		RESISTOR, 6.2K, 1/4W, 5%	R31, R34
27	1		RESISTOR, 3.6K, 1/4W, 5%	R18
28	1		RESISTOR, 2.2K, 1/4W, 5%	R1
29	2		RESISTOR, 1K, 1/4W, 5%	R5, R57
30	8		RESISTOR, 27K, 1/4W, 5%	R47 THRU R54
31	2		RESISTOR, 1M, 1/4W, 5%	R44, R46
32	2		RESISTOR, 150K, 1/4W, 5%	R16, R17

EXPRESSION BOARD ASSEMBLY

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
33	2	PT15YB10K	POTENTIOMETER, 10K	R6, R7
34	6	RADIAL LEAD	CAPACITOR, 10uf, 15V MIN	C2, C3, C7, C12, C18, C19
35	2	AXIAL LEAD	CAPACITOR .1uf, 50V	C23, C20
36	4	AXIAL LEAD	CAPACITOR, .01uf, 50V	C5, C6, C16, C21
37	1	AXIAL LEAD	CAPACITOR, .068uf, 50V, 20%	C9
38	1	RADIAL LEAD	CAPACITOR, 470pf, 15V, 20%	C10
39	31	100-10B004-1	PIN, .045 SQ	
40	1	P15B	POTENTIOMETER, 3K	R38
41	5	RADIAL LEAD	CAPACITOR, 1uf, 15V MIN	C1, C14, C4, C15, C8
42	1	100-11A016-1	MICROPHONE	
43	5		RESISTOR, 4.7K, 1/4W, 5%	R8, R9, R10, R28, R36
44	1	4012B	INTEGRATED CIRCUIT	U17
45	2	AXIAL LEADS	CAPACITOR, .01uf, 50V	C11, C13
46	1	RADIAL LEAD	CAPACITOR, .005uf, -20% +60%	C22
47	1		RESISTOR, 51K, 1/4W, 5%	R55
48	1	2222-428-2-1003	CAPACITOR, .01uf, 63V, 5%	C17
49	A/R		SOLDER	
50	1		RESISTOR, 2.7K, 1/4W, 5%	R56

PT-100 CASSETTE RECORDER - REPRODUCER

(Part Number PT-100 or refurbished, PT-100W)

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
P101	75061251P0	JUMPER	1
001C*	4385064016	CASE	1
001F	4385160010	BRACKET	1
001H	4385052010	COUNTER	1
001U	4385809010	CUSHION	1
002C*	4385251010	BADGE	1
002F	5128030880	B.H. TAP. SCREW	3
002H	4384264020	BELT	1
002N	4367105700	CHASSIS	1
002P	4378104010	RETAINER	1
002U	4385809020	CUSHION	1
003C*	4385063014	ESCUTCHEON	1
003H	4384055010	COLLAR	2
003N	4367105015	CHASSIS	1
003P*	4378354010	LEVER	6
003U	4385804010	SLEEVE	1
004C*	4385063020	ESCUTCHEON	1
004F	51042604A0	F.H.M. SCREW	2
004H	51060316A9	P.H.M. SCREW	2
004N	4367112030	SHAFT	2
004P	4378112010	SHAFT	1
005C*	4385063040	ESCUTCHEON	1
005F	51102604A0	B.H.M. SCREW	2
005N	4367112040	SHAFT	1
006C*	4385063050	ESCUTCHEON	1
006N	4367112050	SHAFT	1
007C*	4385063060	ESCUTCHEON	1
007U	4385805010	MASTER CARTON	6
008N	4367112220	SHAFT	1
009N	4367112084	SHAFT	1
009U	4385807010	REINFORCING	6
010F	51280303B0	B.H. TAP. SCREW	2
010N	3367106020	SUSTAINER	1
010P	51300308B0	P.H. TAP. SCREW	2
011C*	3347274010	REFLECTOR	1
011F	51280312B0	B.H. TAP. SCREW	4
011N	4367101020	SUPPORT	1
012C*	3412056080	BUFFER	2
012N	4367112190	SHAFT	3
012U	9012535010	POLYETHY BAG	1
013C*	4385257020	LID	1
013N	4367112200	SHAFT	1
013U	9013025010	POLYETHY BAG	1
014C	4167115010	SPRING	1
015C*	4385063030	ESCUTCHEON	1
015N	4367354700	LEVER	1

* Assembly

PT-100 CASSETTE RECORDER - REPRODUCER

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
015P	64000400R0	RG RING, F	2
015U	9522815010	SERIAL NO CARD	1
016N	4367354012	LEVER	1
016U	51480306S9	F. WASHER SCREW	4
017N	4367254010	PIN	1
017U	9010508010	POLYETHY BAG	1
020C*	4385353010	RING	1
020F	4385271010	HOLDER	1
020P*	4167270010	BUTTON	1
021P*	4167270020	BUTTON	1
022P*	4167270030	BUTTON	1
023P*	4167270040	BUTTON	1
024P*	4167270050	BUTTON	1
025C*	4656154050	KNOB	1
025F	4385271020	HOLDER	1
025N	4367354720	LEVER	1
025P	4167270060	BUTTON	1
026C	4656053010	COVER	1
026N	4367354030	LEVER	1
027C	4123154030	KNOB	3
027N	4367254010	PIN	1
030F	4385160020	BRACKET	1
031F	51280312B0	B.H. TAP. SCREW	2
032F	51100304A9	B.H.M.SCREW	2
035N	4367354730	LEVER	1
036N	4367354042	LEVER	1
037N	4367254010	PIN	1
045N	4367354740	LEVER	1
046N	4367354050	LEVER	1
047N	4367254010	PIN	1
051D*	4385257014	LID	1
052D*	4385063070	ESCUTCHEON	1
060D	51280330B0	B.H. TAP. SCREW	1
061D	51280340B0	B.H. TAP. SCREW	1
061N	4367354070	LEVER	1
070N	4367354060	LEVER	1
071N	4367354090	LEVER	1
072N	4367354120	LEVER	1
076N	4367002700	ARM	1
077N	4367002030	ARM	1
078N	4367112100	SHAFT	1
079N	1861255010	PINCH ROLLER	1
085N	4367051700	GUIDE	1
086N	4367051010	GUIDE	1
087N	4367002060	ARM	1
088N	4367112160	SHAFT	1

* ASSEMBLY

PT-100 CASSETTE RECORDER - REPRODUCER

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
095N	4367354760	LEVER	1
096N	4367354100	LEVER	1
097N	4367254030	PIN	1
098N	4367001520	IDLER	1
110N	4367004700	TABLE	1
111N	4367004500	TABLE	1
112N	4367004012	TABLE	1
113N	4367353050	RING	1
114N	4367061020	CLUTCH	2
115N	4367266020	WHEEL	1
116N	4367115010	SPRING	1
117N	59050802G9	WASHER	1
118N	4367272012	POLE	1
119N	4367004023	TABLE	1
120N	4367115300	SPRING	1
121N	4367067020	CAP	1
122N	4367259010	BUSHING	1
130N	4367004710	TABLE	1
131N	4367004030	TABLE	1
132N	4367115183	SPRING	1
133N	4367067020	CAP	1
134N	4367259010	BUSHING	1
141N	4367002020	ARM	1
142N	4367112122	SHAFT	1
143N	4367001510	IDLER	1
146N	59020805G9	WASHER	1
147N	4367118040	SPACER	1
175N	4367002720	ARM	1
176N	4367002070	ARM	1
177N	4367001533	IDLER	1
180N	4367254050	PIN	1
185N	4367354770	LEVER	1
186N	4367354130	LEVER	1
187N	4367258020	HOOK	1
188N	4367112143	SHAFT	1
189N	4367115330	SPRING	1
190N	4367118030	SPACER	1
195N	4367002050	ARM	1
196N	4367115130	SPRING	1
201N	4367354080	LEVER	1
202N	4367115070	SPRING	1
212N	4367264030	BELT	1
224N	4367115060	SPRING	1
225N	4367115170	SPRING	1
226N	4367112180	SHAFT	1
227N	4367051040	GUIDE	1
228N	4367055020	COLLAR	2
229N	51280312B0	B.H. TAP. SCREW	2

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
235N	4367067010	CAP	2
236N	4367263010	BRAKE	2
240N	51610205A0	SET SCREW, F.P.	1
241N	4367259020	BUSHING	3
242N	4367112150	SHAFT	3
245N	51382606P0	P.H. TAP. SCREW	1
250N	4367115040	SPRING	1
252N	4367115080	SPRING	1
253N	4367115310	SPRING	1
258N	4367056040	BUFFER	1
259N	4367056030	BUFFER	1
260N	4367115240	SPRING	1
261N	4367115090	SPRING	1
262N	4367115120	SPRING	1
263N	4367115250	SPRING	1
264N	4367115340	SPRING	1
265N	4367115270	SPRING	1
266N	4367115280	SPRING	2
268N	4367115210	SPRING	1
275N	51300308B0	P.H. TAP. SCREW	1
280N	61020010T0	BALL	5
285N	64002500R0	RG RING, E	2
286N	64001500R0	RG RING, E	2
287N	64000300R0	RG RING, E	4
290N	59020402G9	WASHER	2
295N	59264702G9	WASHER	1
300N	4367354110	LEVER	1
305N	4367058010	GEAR	1
306N	59046501G9	WASHER	1
310N	4367056050	BUFFER	2
400N	4367354750	LEVER	1
401N	4367354142	LEVER	1
402N	4367254020	PIN	1
403N	4367115210	SPRING	1
404N	4367112130	SHAFT	1
405N	4367054030	CAM	1
406N	4367115140	SPRING	1
407N	59020805G9	WASHER	1
408N	64001500R0	RG RING, E	1
410N	4367254040	PIN	1
411N	4367160022	BRACKET	1
705N*	4385160052	BRACKET	1
706N*	4385112070	SHAFT	2
707N	4385058030	GEAR	1
708N	4385112062	SHAFT	1
709N	64001500R0	RG RING, E	2
710N	4385160062	BRACKET	1

* Assembly

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
711N	64002500R0	RG. RING, E	1
712N	51280308B0	B.H. TAP. SCREW	1
716N	51340308A0	F.H. TAP. SCREW	1
717N	51100306A9	B.H.M. SCREW	2
718N	4385354040	LEVER	1
725N	4385058010	GEAR	1
726N	5311020380	HEXAGON NUT	1
727N	54010300E0	FLAT WASHER, S.	1
728N	54040202B0	SPRING WASHER	1
730N	4385058050	GEAR	1
731N	4385118010	SPACER	1
733N	4385354050	LEVER	1
734N	4385115010	SPRING	1
735N	4385259010	BUSHING	1
736N	51100204A0	B.H.M. SCREW	2
737N	4385115060	SPRING	1
738N	3048254020	PIN	1
739N	3444118070	SPACER	1
753N	4385112050	SHAFT	1
754N	4385154010	KNOB	1
755N	4385115050	SPRING	1
764N	51102606A0	B.H.M. SCREW	1
765N	54022601A0	FLAT WASHER, P.	1
770N	4385055010	COLLAR	1
771N	51040205A0	F.H.M. SCREW	1
810N	4378354700	LEVER	1
811N	4367354020	LEVER	1
812N	4367254010	PIN	1
813N	4378115010	SPRING	1
820N	4367054040	CAM	1
821N	4367054050	CAM	1
840N	4367002040	ARM	1
845N	4367258010	HOOK	1
846N	4378115020	SPRING	1
850N	4385262010	PULLEY	1
880N	62021030W0	LUG	1
890N	4367115290	SPRING	1
900T	9560000090	HANG TAG	1
901D	4385265010	INDICATOR	1
902N	4367001700	IDLER	1
903N	4367002010	ARM	1
904N	4367106010	SUSTAINER	1
905N	4367112010	SHAFT	1
906N	4367266030	WHEEL	1
907N	4367061010	CLUTCH	1
908N	4367001500	IDLER	1
911N	4367115110	SPRING	1
911T	9660000010	QC CARD	1
912N	4367262030	PULLEY	1

PT-100 CASSETTE RECORDER - REPRODUCER

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
913N	59020402G9	WASHER	2
914N	64001500R0	RG RING, E	1
917T	3906854020	GUARANTEE CARD	1
918T	2876851030	INSTRUCTIONS	1
919T	9630000170	GUARANTEE CARD	1
920N	4367273500	FLYWHEEL	1
925N	4385264010	BELT	1
930N	4367104700	RETAINER	1
931N	4367106030	SUSTAINER	1
932N	4367104010	RETAINER	1
942N	3483164020	ADJUSTER	1
946N	51300310B0	P.H. TAP. SCREW	2
950N	4380115080	SPRING	1
953N	4385112080	SHAFT	1
955N	4367115280	SPRING	1
961N*	4385105013	CHASSIS	1
962N*	4385101013	SUPPORT	1
964N	4385160070	BRACKET	1
965N	64000300R0	RG RING, E	1
967N	4385160040	BRACKET	1
968N	51100210A0	B.H.M. SCREW	1
969N	51100208A0	B.H.M. SCREW	1
970N	51100206A0	B.H.M. SCREW	1
971N	51100204A0	B.H.M. SCREW	1
972N	51100205A0	B.H.M. SCREW	1
975N	4385115020	SPRING	1
976N	51380206P0	P.H. TAP. SCREW	1
H001	LH41551010	REC/PLAY HEAD	1
H002	LH31000320	ERASE HEAD	1
J002	BY01240010	JACK	1
J004	YJ01001140	JACK	1
M001	MM11200070	D.C. MOTOR	1
Q001	HI10001060	L.E.D.	1
Q002	HI10004030	L.E.D.	1
S001	SM01010640	MINI SWITCH	1
S002	SM01010520	MINI SWITCH	1
S003	SC02020230	SWITCH	1
C101	EA22701690	ELECT CAP	1
C102	EA47502590	ELECT CAP	1
C103	DD15390040	CERAMIC CAP.	1
C104	DK18104010	CERAMIC CAP	1
C105	DD16101010	CERAMIC CAP.	1
C106	DK18104010	CERAMIC CAP.	1
C107	DK16472010	CERAMIC CAP.	1
C108	EA47502590	ELECT CAP	1
C109	DK16222010	CERAMIC CAP.	1
J101	YP10001790	PLUG	1
P100	ZZ43850210	P.W. BOARD	1

* Assembly

PT-100 CASSETTE RECORDER - REPRODUCER

REF. DESIG.	PARTS NO.	DESCRIPTION	QTY. REQ.
Q101	HC10003090	IC	1
Q102	HC10003090	IC	1
R101	RT05102140	RESISTOR	1
R102	RT05511140	RESISTOR	1
R104	RK07510020	VARIABLE RESIST	1
R105	RT05154140	RESISTOR	1
R106	RT05184140	RESISTOR	1
R107	RT05102140	RESISTOR	1
R108	RT05624140	RESISTOR	1
R109	RT05153140	RESISTOR	1
R110	RT05624140	RESISTOR	1
R111	RT05153140	RESISTOR	1
R112	RT05624140	RESISTOR	1
R113	RT05102140	RESISTOR	1
R114	RT05121140	RESISTOR	1
R115	RT05681140	RESISTOR	1
R116	RT05152140	RESISTOR	1
R117	RT05512140	RESISTOR	1
R118	RK01030330	VARIABLE RESIST	1
R119	RK05020240	VARIABLE RESIST	1
R120	RT05561140	RESISTOR	1
R121	RT05102140	RESISTOR	1
R125	RT05222140	RESISTOR	1
R126	RT05182140	RESISTOR	1
R127	RT05751140	RESISTOR	1
R128	RA03020030	TRIMMING RESIST	1
R129	RA03020030	TRIMMING RESIST	1
R130	RT05751140	RESISTOR	1
S101	SS06020360	SLIDE SWITCH	1

PRINTED WIRING ASSEMBLY PLAYBACK BOARD

(Part Number 100-04D0-111 or refurbished, 100-04D0-11W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05D011-1	P.W. BOARD	
2	4		RESISTOR, 22K, 1/4W, 5%	R6, R10, R94, R93
3	10		RESISTOR, 10K, 1/4W, 5%	R7, R16, R17, R38, R40, R41, R48, R66, R67, R77
4	11		RESISTOR, 1K, 1/4W, 5%	R2, R3, R13, R14, R33, R34, R35, R98, R88, R90, R103
5	4	PT 15YBZ0K or EQ	POTENTIOMETER 20K	R37, R68, R72, R82
6	1	PT15YB50K or EQ	POTENTIOMETER 50K	R9
7	1		RESISTOR, 39K 1/4W, 5%	R20
8	1		RESISTOR, 120K, 1/4W, 5%	R52
9	11		RESISTOR, 2.2K, 1/4W, 5%	R1, R32, R53, R78, R81, R85, R87, R89, R95, R99, R100
10	2		RESISTOR, 4.7K, 1/4W, 5%	R54, R102
11	2		RESISTOR, 3.3K, 1/4W, 5%	R56, R51
12	12		RESISTOR, 100K, 1/4W, 5%	R39, R42, R47, R69, R57, R58, R59, R61, R62, R64, R91, R92
13	1		RESISTOR, 100, 1/4W, 5%	R55
14	2		RESISTOR, 1.5M, 1/4W, 5%	R22, R28
15	2		RESISTOR 680K, 1/4W, 5%	R23, R29
16	2		RESISTOR, 390K, 1/4W, 5%	R24, R30
17	6		RESISTOR, 220K, 1/4W, 5%	R25, R31, R36, R45, R40, R65
18	1		RESISTOR, 47K, 1/4W, 5%	R84
19	2		RESISTOR, 8.2K 1/4W, 5%	R46, R50
20	5		RESISTOR, 510, 1/4W, 5%	R96, R43, R44, R70, R71
21	1		RESISTOR, 33K, 1/4W, 5%	R86
22		DELETED		
23	1		RESISTOR, 220, 1/4W, 5%	R15

PRINTED WIRING ASSEMBLY PLAYBACK BOARD

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
24	64	100-10B004-1	PIN .045 SQ	
25	4	2N5172	TRANSISTOR	Q2 thru Q4, Q6
26	2	2N6076	TRANSISTOR	Q1, Q5
27	9	1N914	DIODE	D3 THRU D11
28	3		RESISTOR, 75K, 1/4W, 5%	R73, R74, R4
29	4	ELECTROLYTIC	CAPACITOR, 47uf, 10V, 20%	C6, C7, C14, C15
30	3	ELECTROLYTIC	CAPACITOR, 10uf, 10V, 20%	C17, C23, C16
31		DELETED		
32	1	74LS14	INTEGRATED CIRCUIT	U14
33	9	CERAMIC, AXIAL	CAPACITOR, 0.1uf, 50V, -20%, +20%	C5, C21, C22, C8, C19, C20, C3, C24, C25
34	1	CERAMIC, AXIAL	CAPACITOR, .001uf, 50V, 10%	C18
35	2	CERAMIC, AXIAL	CAPACITOR, .01uf, 50V, 5%	C2, C9
36		DELETED		
37	7	CERAMIC, AXIAL	CAPACITOR, .01uf, 50V, 20%	C1, C4, C10, C11, C12, C26, C27
38	1	4N37	INTEGRATED CIRCUIT	U11
39	1		RESISTOR, 390, 1/2W, 5%	R26
40	1	74LS86	INTEGRATED CIRCUIT	J28
41	1	74L121	INTEGRATED CIRCUIT	U27
42	1	74LS122	INTEGRATED CIRCUIT	U26
43	2		RESISTOR, 51K, 1/4W, 5%	R60, R63
44	3	LM324 QUAD OP-AMP	INTEGRATED CIRCUIT	U18, U10, U19
45	1	LM339 QUAD COMP.	INTEGRATED CIRCUIT	U6
46	2	74LS30	INTEGRATED CIRCUIT	U16, U8
47	1	74LS04	INTEGRATED CIRCUIT	U4
48	2	74LS00	INTEGRATED CIRCUIT	U5, U3
49	1	74LS73	INTEGRATED CIRCUIT	U9
50	1	74LS20	INTEGRATED CIRCUIT	U1
51	1	7417	INTEGRATED CIRCUIT	U15
52	1	74LS154	INTEGRATED CIRCUIT	U20
53	2	74LS191	INTEGRATED CIRCUIT	U22, U21
54	1	74LS02	INTEGRATED CIRCUIT	U25
55	1	74LS164	INTEGRATED CIRCUIT	U7
56	1	74LS74	INTEGRATED CIRCUIT	U2
57	3	4016B or 4066B	I.C., QUAD BILATERAL SWITCH	U13, U17, U24
58	2	74LS259	INTEGRATED CIRCUIT	U12, U23
59	2		RESISTOR, 3.3m, 1/4W, 5%	R21, R27

PRINTED WIRING ASSEMBLY PLAYBACK BOARD

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
60		DELETED		
61	1	DELETED		
62		DELETED		
63	1		RESISTOR, 470K, 1/4W, 5%	R97
64	1		RESISTOR, 1.3K, 1/4W, 5%	R8
65		DELETED		
66		DELETED		
67	1		RESISTOR, 12K, 1/4W, 2%	R80
68	1	PT15YB10K	POTENTIOMETER, 10K	R19
69	2		RESISTOR, 27K, 1/4W, 5%	R12, R18
70	1		RESISTOR, 27K, 1/4W, 2%	R79
71	1		RESISTOR, 1K, 1/4W, 2%	R76
72	1		RESISTOR, 2.2K, 1/4W, 2%	R83
73	3		RESISTOR, 10, 1/4W, 5%	R5, R75, R101

P.W. BOARD ASSEMBLY END DRIVER

(Part Number 100-04D0-031 or refurbished, 100-04D0-03W)

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1	1	100-05D003-1	P.W. BOARD	
2	A/R	SOLDER		
3	42	BARE STRAP 1/2"	WIRE, AWG #22	
4	76	100-10B004-1	PIN, .045 SQ	
5	6	#6 x 1/4 LG	METAL SCREW, PAN HD, OR SCREW STICK	
6	1	350209-1	CONNECTOR	J2
7	1	ECE-A250V3R3	CAPACITOR, 3.3uf, 250V	C1
8	4	CERAMIC	CAPACITOR, 1uf, 50V, -20, +80	C2, C3, C4, C5
9	65	1N4004	DIODE	D1 THRU D65
10	4	74LS259	INTEGRATED CIRCUIT	U1 THRU U4
11	8	74LS08	INTEGRATED CIRCUIT	U5 THRU U12
12	32	100-02A159-1	TRANSISTOR	Q1 THRU Q32
13	32		RESISTOR, 1K, 1/4W, 5%	R1 THRU R32
14	1		RESISTOR, 10, 1/2W, 5%	R33
15		DELETED		
16	3	100-02B011-1	BRACKET	

P.W. BOARD ASSEMBLY CENTER DRIVER

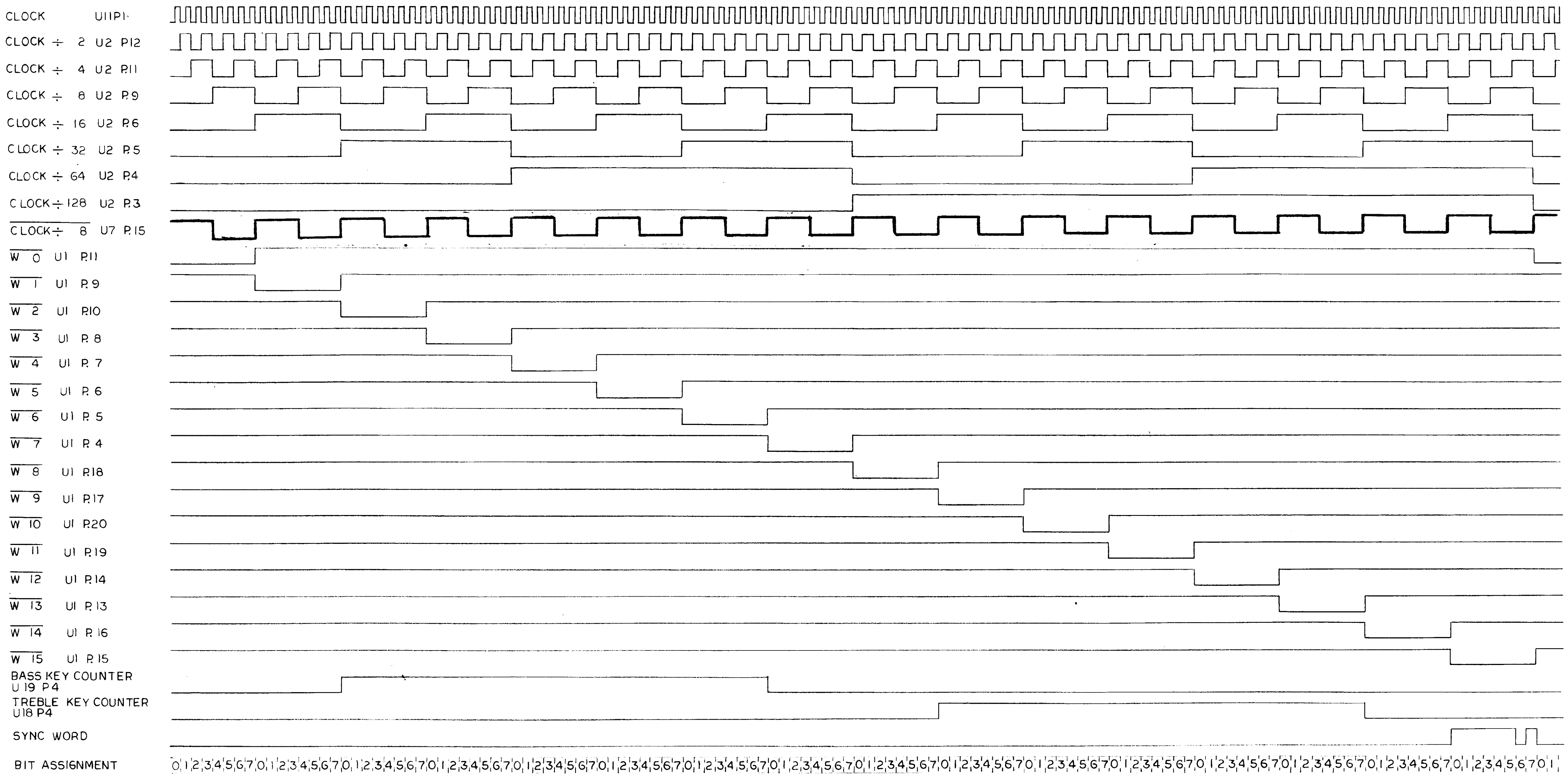
(Part Number 100-04D0-041 or refurbished, 100-04D0-04W

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION
1.	1	100-05D004-1	P.W. BOARD	
2.	A/R		SOLDER	
3.	16		RESISTOR, 1K, 1/4W 5%	R1 THRU R16
4.	33	1N4004	DIODE	D1 THRU D33
5.	16	100-02A159-1	TRANSISTOR	Q1 THRU Q16
6.	2	74LS259	INTEGRATED CIRCUIT	U1 THRU U2
7.	8	74LS08	INTEGRATED CIRCUIT	U3 THRU U6
8.	1	ECE-A250V3R3	CAPACITOR, 3.3uf, 250V	C1
9.	1	CERAMIC	CAPACITOR, .1uf, 50V, +80%/-20%	C2
10.	26	BARE STRAP ½"	WIRE, AWG #22	
11.	45	100-10B004-1	PIN, .045 SQ.	
12.	3	350209-1	CONNECTOR	J2, J3, J4
13.	2	74LS02	INTEGRATED CIRCUIT	U7 THRU U8
14.	2	100-02B011-1	BRACKET	
15.	1		RESISTOR, 10, 1/2W, 5%	R17
16.			DELETE	
17.	4	#6 X 1/4 LG	METAL SCREW, PAN HD OR SCREW STICK	

FIGURE 4
BIT ASSIGNMENT MAP

BIT	FUNCTION	BIT	FUNCTION	BIT	FUNCTION
1.	Soft Pedal	44.	Note 32 E	87.	Note 59 G
2.	Sustain Pedal	45.	Note 33 F	88.	Note 60 G#
3.	Not used	46.	Note 34 F#	89.	Note 61 A
4.	Bass Intensity 1	47.	Note 35 G	90.	Note 62 A#
5.	Bass Intensity 2	48.	Note 36 G#	91.	Note 63 B
6.	Bass Intensity 3	49.	Note 37 A	92.	Note 64 C
7.	Bass Intensity 4	50.	Note 38 A#	93.	Note 65 C#
8.	Bass Intensity 5	51.	Note 39 B	94.	Note 66 D
9.	Not used	52.	Note 40 C	95.	Note 67 D#
10.	Not used	53.	Note 41 C#	96.	Note 68 E
11.	Not used	54.	Note 42 D	97.	Note 69 F
12.	Not used	55.	Note 43 D#	98.	Note 70 F#
13.	Not used	56.	Note 44 E	99.	Note 71 G
14.	Not used	57.	Not used	100.	Note 72 G#
15.	Not used	58.	Not used	101.	Note 73 A
16.	Not used	59.	Not used	102.	Note 74 A#
17.	Note 5 C#	60.	Not used	103.	Note 75 B
18.	Note 6 D	61.	Not used	104.	Note 76 C
19.	Note 7 D#	62.	Not used	105.	Note 77 C#
20.	Note 8 E	63.	Not used	106.	Note 78 D
21.	Note 9 F	64.	Not used	107.	Note 79 D#
22.	Note 10 F#	65.	Cont. Bit 1	108.	Note 80 E
23.	Note 11 G	66.	Cont. Bit 2	109.	Note 81 F
24.	Note 12 G#	67.	Not used	110.	Note 82 F#
25.	Note 13 A	68.	Treb Intensity 1	111.	Note 83 G
26.	Note 14 A#	69.	Treb Intensity 2	112.	Note 84 G#
27.	Note 15 B	70.	Treb Intensity 3	113.	Not used
28.	Note 16 C	71.	Treb Intensity 4	114.	Not used
29.	Note 17 C#	72.	Treb Intensity 5	115.	Not used
30.	Note 18 D	73.	Note 45 F	116.	Not used
31.	Note 19 D#	74.	Note 46 F#	117.	Not used
32.	Note 20 E	75.	Note 47 G	118.	Not used
33.	Note 21 F	76.	Note 48 G#	119.	Not used
34.	Note 22 F#	77.	Note 49 A	120.	Not used
35.	Note 23 G	78.	Note 50 A#	121.	Sync Bit 1
36.	Note 24 G#	79.	Note 51 B	122.	Sync Bit 2
37.	Note 25 A	80.	Note 52 C	123.	Sync Bit 3
38.	Note 26 A#	81.	Note 53 C#	124.	Sync Bit 4
39.	Note 27 B	82.	Note 54 D	125.	Sync Bit 5
40.	Note 28 C	83.	Note 55 D#	126.	Sync Bit 6
41.	Note 29 C#	84.	Note 56 E	127.	Sync Bit 7
42.	Note 30 D	85.	Note 57 F	128.	Sync Bit 8
43.	Note 31 D#	86.	Note 58 F#		

FIGURE I RECORD SYSTEM TIMING DIAGRAM



NOTES:

UNLESS OTHERWISE SPECIFIED
1. BREAK ALL SHARP CORNERS .015 MAX.
2. SURFACE ROUGHNESS 63 MICROINCH R.M.S. MAX.
3. DIAMETERS TO BE CONCENTRIC WITHIN .005 T.I.R.
4. FILLET RADIUS .010 MAX.
5. THREADS – CLASS 2

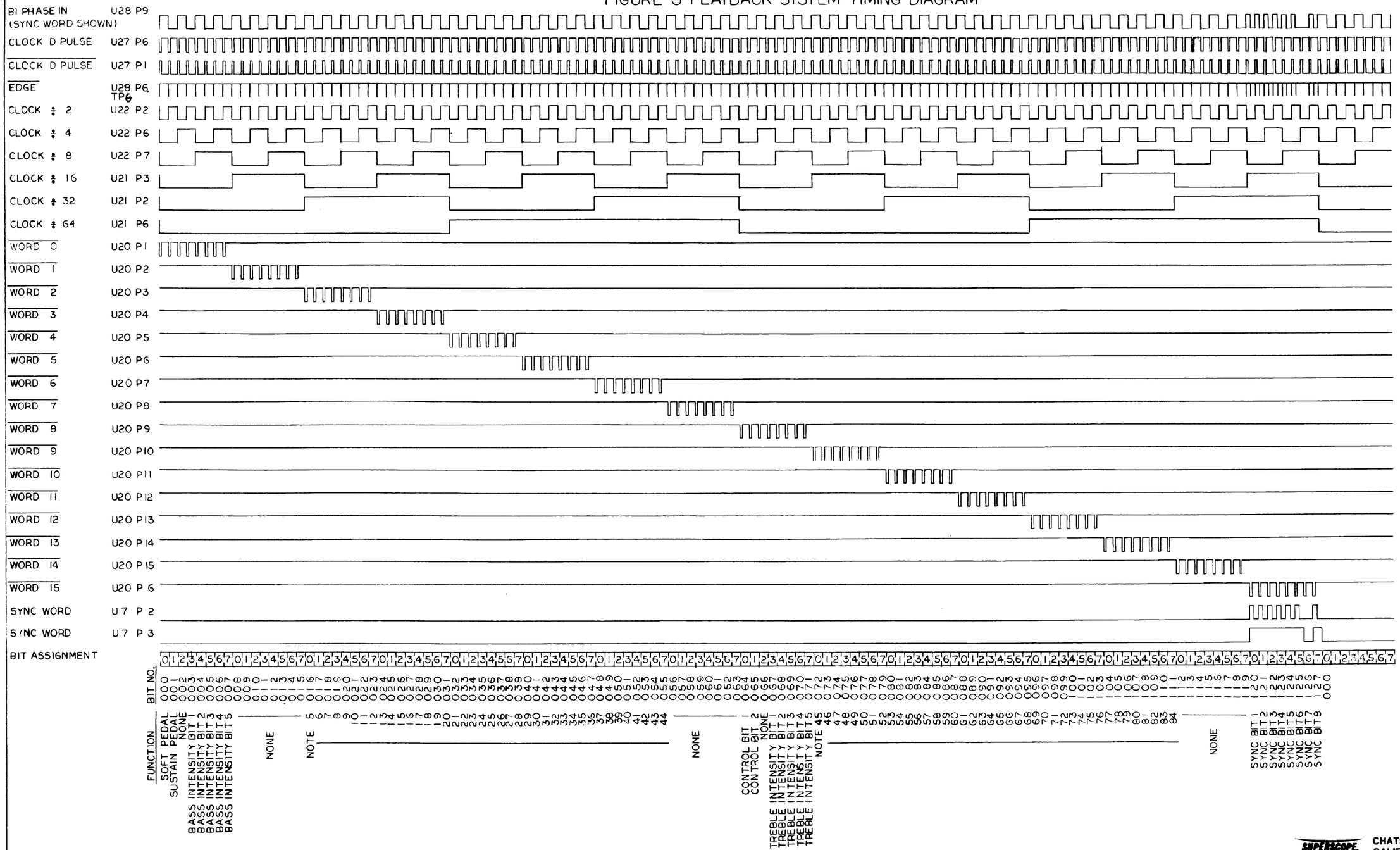
TOLERANCES UNLESS OTHERWISE NOTED
ANGLES ±0° 30′ FRACTIONS ± 1/32 DECIMALS .XX ±.020 .XXX ±.010
DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING

DRAWN BY Merlyn Morgan DATE 3/79
CHECKED
APPROVED
PROJ. ENG. Merlyn Morgan

SUPERSCOPE. CHATSWORTH, CALIFORNIA

DWG. TITLE RECORDING SYSTEM TIMING DIAGRAM

FIGURE 3 PLAYBACK SYSTEM TIMING DIAGRAM



NOTES :

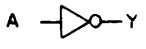
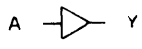
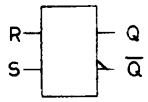
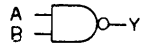
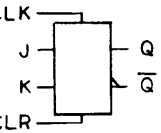
SUPERSCOPE. CHATSWORTH CALIFORNIA

DWG TITLE: TIMING DIAGRAM, PLAYBACK SYSTEM

RELATED DWGS | DWG NO | REV | SCALE | SHEET OF

SYM.	DESCRIPTION	BY/MN	DATE	APPR'D.

FIGURE 7
LOGIC DIAGRAMS, TRUTH TABLES

FUNCTION		TRUTH TABLE	FUNCTION		TRUTH TABLE
AND GATE		A 0 0 1 1 B 0 1 0 1 Y 0 0 **0** 1	INVERTER		A C 1 Y 1 0
OR GATE		A 0 1 0 1 B 0 0 1 1 Y 0 1 1 1	X-OR		A 0 1 0 1 B 0 0 1 1 Y 0 1 1 C
BUFFER		A=Y	RESET-SET FLIP FLOP		S 0 1 0 1 R C C 1 1 Q Z 1 0 X $\bar{Q}$ Z 0 1 X
NAND GATE		A 0 1 0 1 B 0 0 1 1 Y 1 1 1 0	J-K FLIP FLOP		CLR CLK J K Q $\bar{Q}$ 0 X X X 0 1 1 ↓ 0 0 Q0 $\bar{Q}$0 1 ↓ 0 1 0 1 1 ↓ 1 0 1 0 1 ↓ 1 1 TOGGLE 1 ↓ X X Q0 $\bar{Q}$0
NOR GATE		A 0 1 0 1 B 0 0 1 1 Y 1 0 0 0			

NOTE: DEFINATIONS
Z=STAYS SAME
X=DONT CARE
0=FALSE=LOW
1=TRUE=HIGH

ITEM	PART NO.	DESCRIPTION
REQ'D. PER ASSY.		LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
1. BREAK ALL SHARP CORNERS .015 MAX.
2. SURFACE ROUGHNESS 63 MICROINCH R. M. S. MAX.
3. DIAMETERS TO BE CONCENTRIC WITHIN .005 T. I. R.
4. FILLET RADIUS .010 MAX.
5. THREADS – CLASS 2

TOLERANCES UNLESS OTHERWISE NOTED
ANGLES ±0° 30' FRACTIONS ± 1/32 DECIMALS .XX±.020 .XXX±.010

DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING
DRAWN BY Marilyn Morgan DATE 4/79
CHECKED
APPROVED
PROJ. ENG.

MATERIAL
FINISH

DASH NO.	NEXT ASSY.	MODEL NO.
APPLICATION		

SUPERSCOPE CHATSWORTH, CALIFORNIA

DWG. TITLE LOGIC DIAGRAMS & TRUTH TABLES

RELATED DWGS. DWG. NO. REV

SCALE SHEET OF

SS-MAR 0168

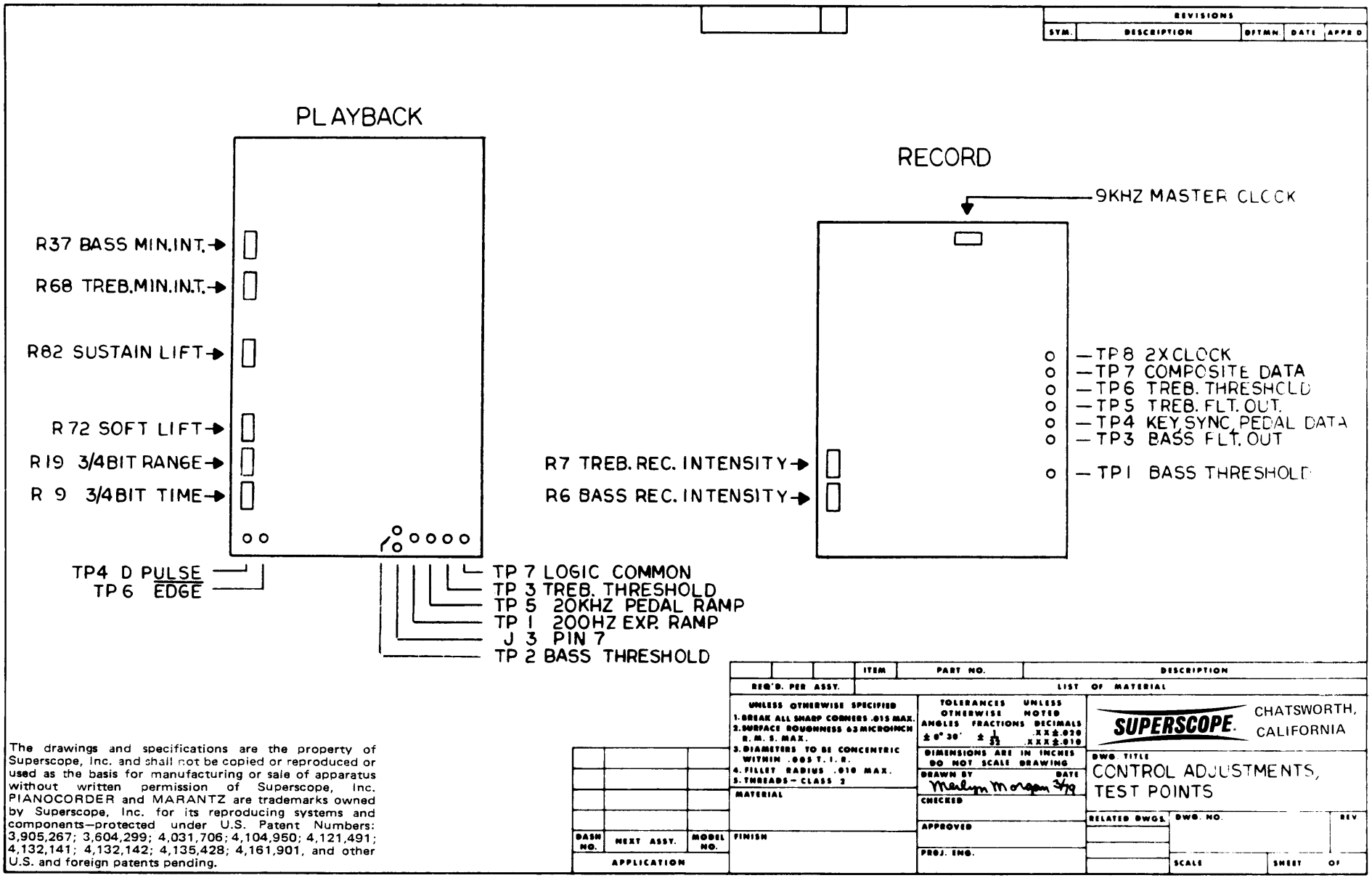


FIGURE 10

FIGURE 12-A

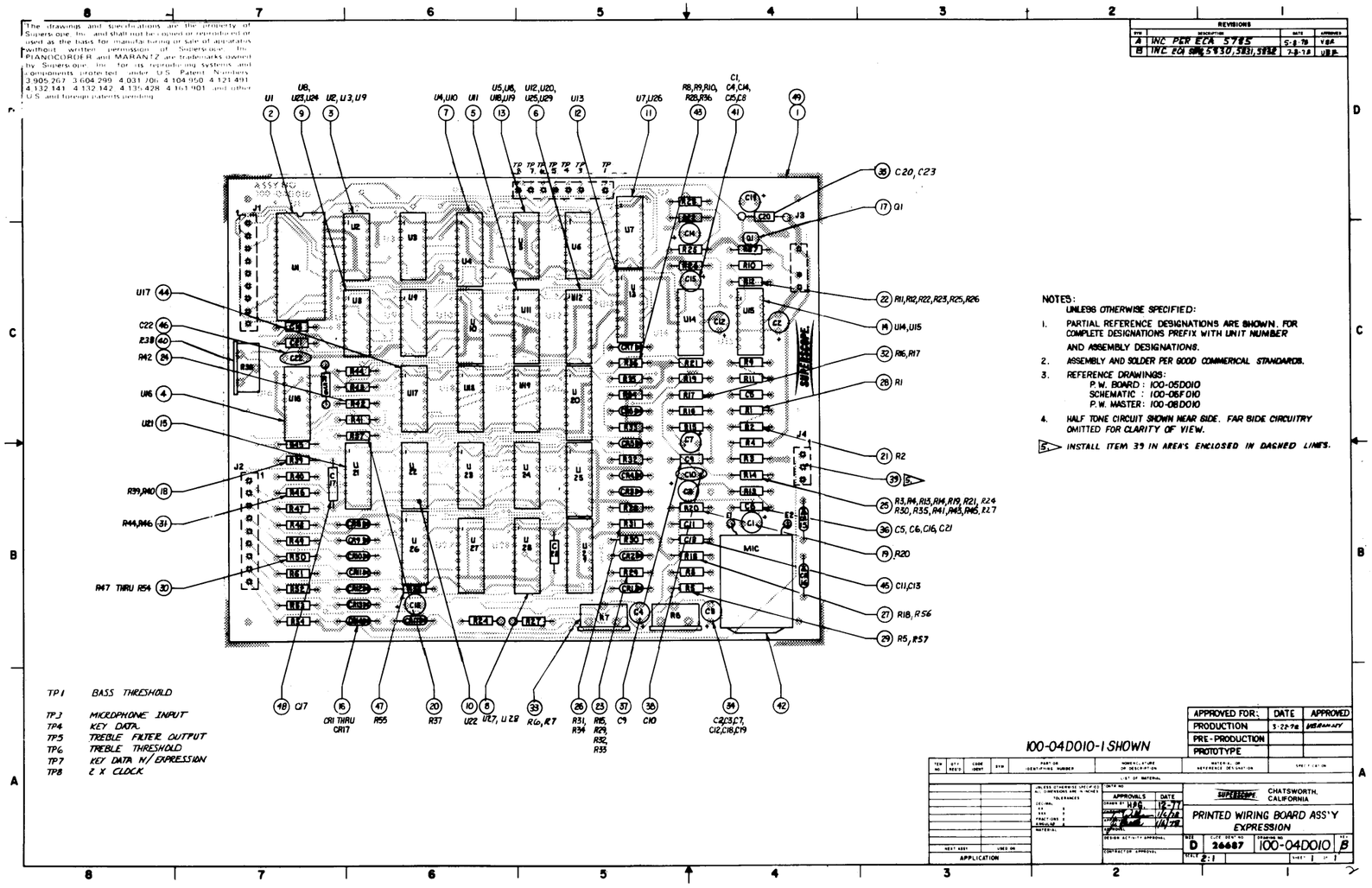
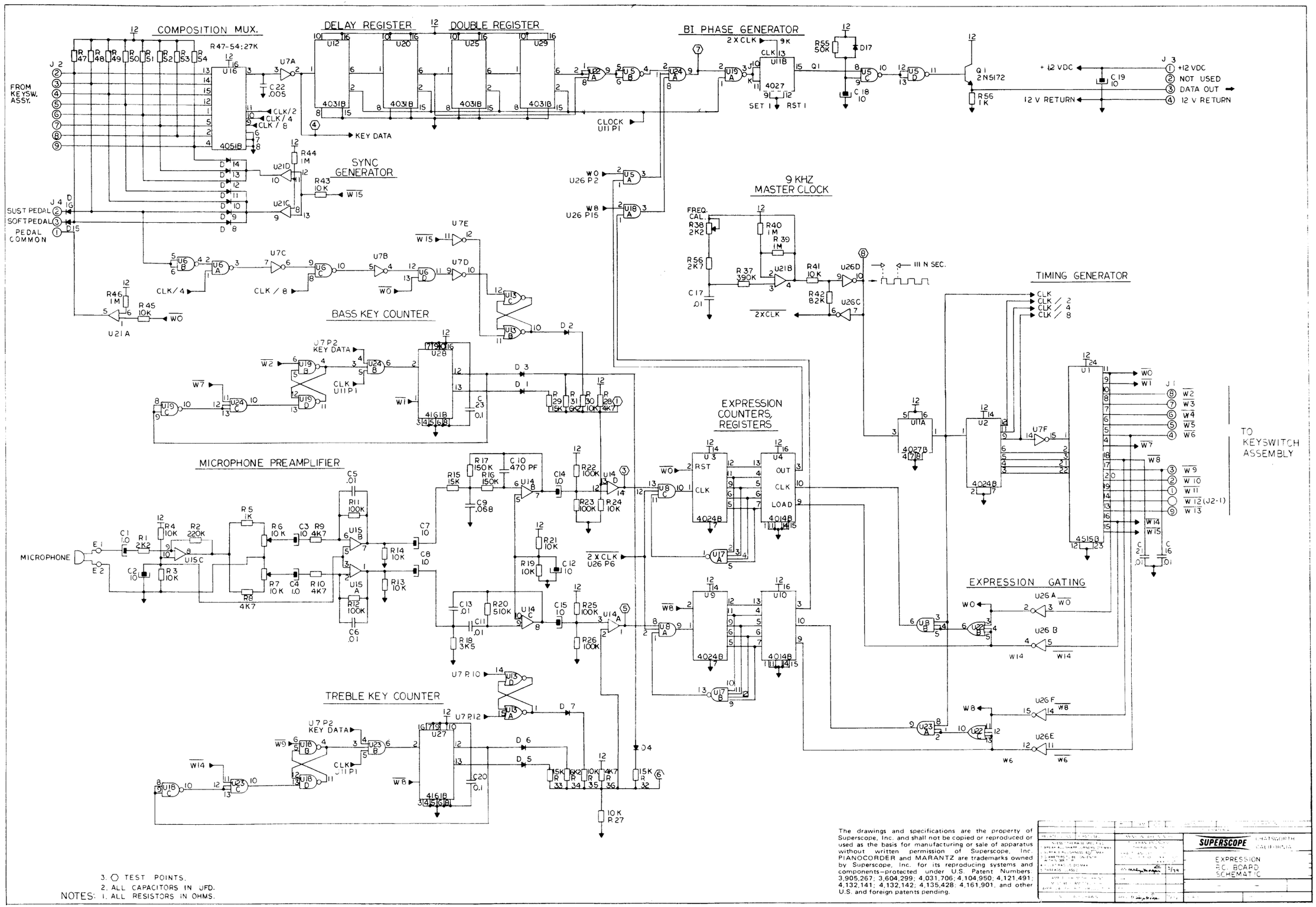

REVISIONS
A INC PER ECA 5785 5-8-78 VGA
B INC PER ECA 5829,5430,5831,5832 7-28-78 WBP
U1 U8, U25,U24 U2,U3,U9 U4,U10 U11 U5,U6, U18,U19 U12,U20, U25,U29 U13 U7,U26 R8,R9,R10, R28,R36 C1, C4,C14, C15,C18 49
C20, C23
Q1
R11,R12,R22,R23,R25,R26
U14,U15
R16,R17
R1
R2
R3,R4,R15,R14,R19,R21, R24 R30, R35, R41, R43, R45, R27
C5, C6, C16, C21
R20
C11,C13
R18, R56
R5, R57
U17 C22 Z38 R42 U16 U21 R39,R40 R44,R46 R47 THRU R54
C17
CR1 THRU CR17
R55
R37
U22 U27, U29
R6, R7
R31, R34
R16, R29, R32, R33
C9
C10
C2,C3,C7, C12,C18,C19
42
TP1 BASS THRESHOLD
TP3 MICROPHONE INPUT
TP4 KEY DATA.
TP5 TREBLE FILTER OUTPUT
TP6 TREBLE THRESHOLD
TP7 KEY DATA W/ EXPRESSION
TP8 2 X CLOCK
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICAL STANDARDS.
3. REFERENCE DRAWINGS:
P.W. BOARD : 100-05D010
SCHEMATIC : 100-05F010
P.W. MASTER: 100-08D010
4. HALF TONE CIRCUIT SHOWN NEAR SIDE. FAR SIDE CIRCUITRY OMITTED FOR CLARITY OF VIEW.
5 INSTALL ITEM 39 IN AREAS ENCLOSED IN DASHED LINES.
100-04D010-1 SHOWN
APPROVED FOR: PRODUCTION; DATE 3-22-78; APPROVED WBRADY
PRE-PRODUCTION
PROTOTYPE
SUPERSCOPE CHATSWORTH, CALIFORNIA
PRINTED WIRING BOARD ASS'Y EXPRESSION
APPROVALS DATE
DRAWN H.P.G. 12-7-77
11-6-78
11-7-78
SIZE D 26687 DRAWING NO. 100-04D010 REV B
SCALE 2:1 SHEET 1 OF 1
APPLICATION
NEXT ASSY USED ON

FIGURE 12B



3. ⬡ TEST POINTS.
2. ALL CAPACITORS IN UFD.
NOTES: 1. ALL RESISTORS IN OHMS.

SUPERSCOPE CHATSWORTH CALIFORNIA

EXPRESSION P.C. BOARD SCHEMATIC

FIGURE 13-A

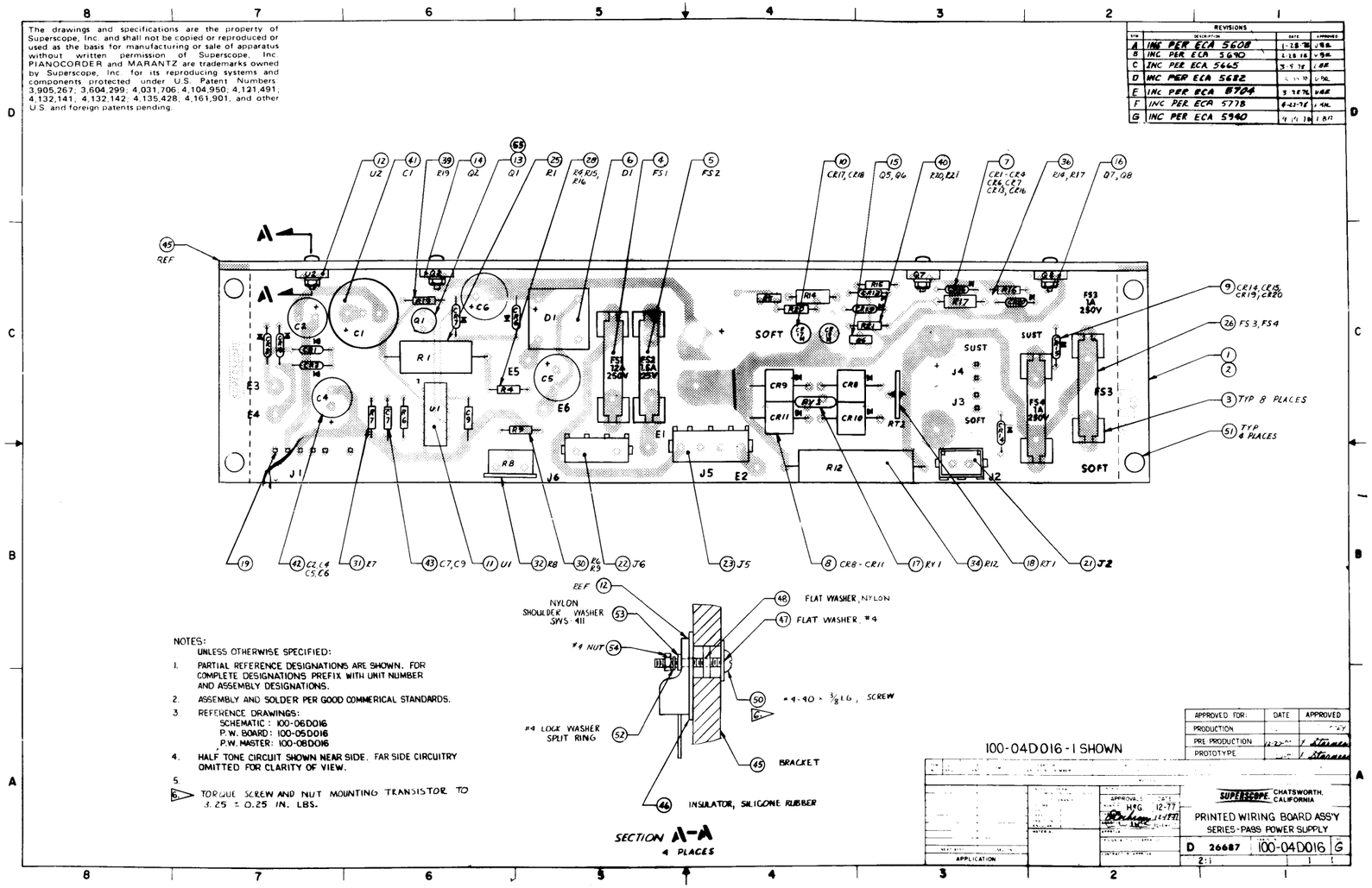
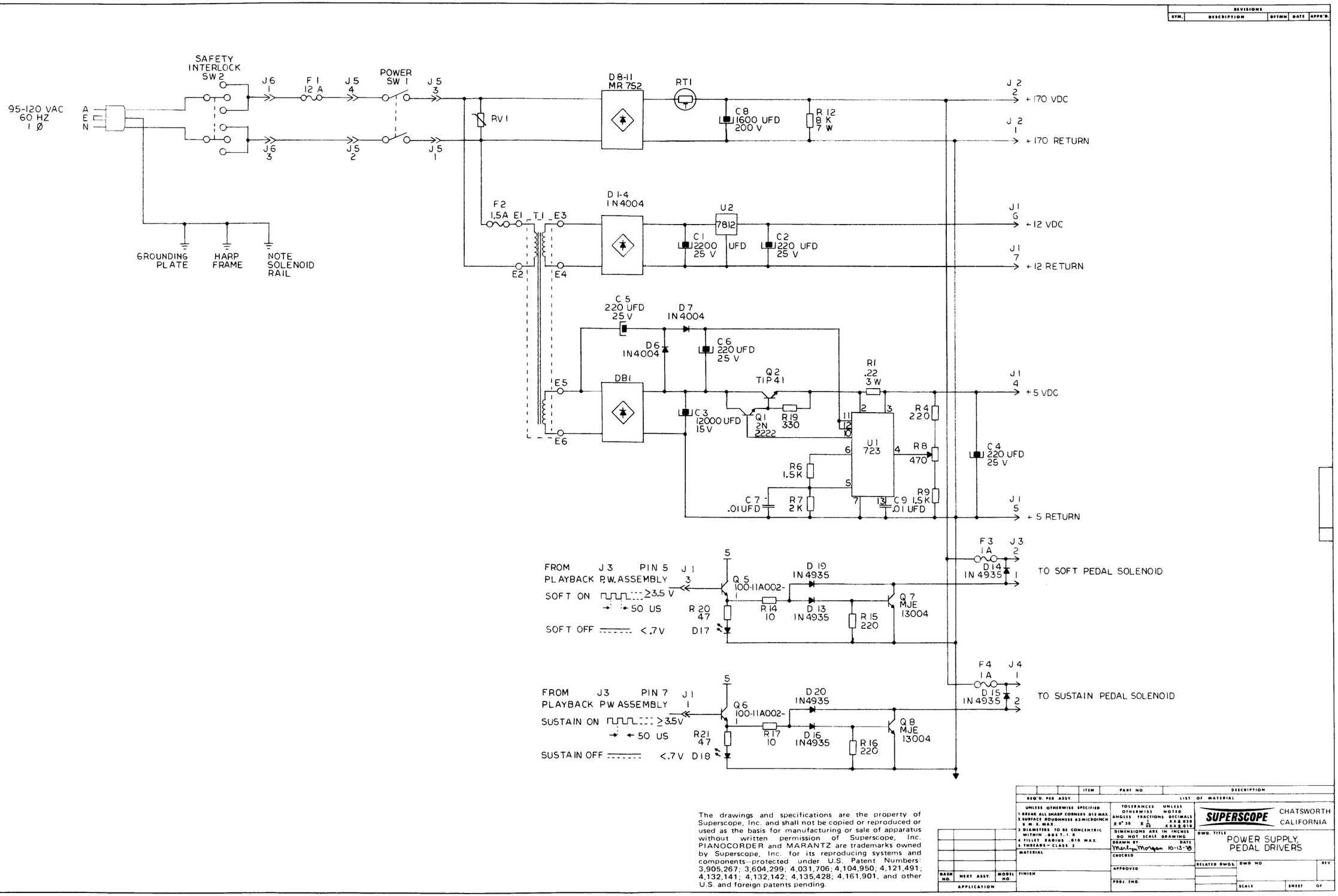

The drawings and specifications are the property of Superscope, Inc. and shall not be copied or reproduced or used as the basis for manufacturing or sale of apparatus without written permission of Superscope, Inc. PIANOCORDER and MARANTZ are trademarks owned by Superscope, Inc. for its reproducing systems and components protected under U.S. Patent Numbers: 3,905,267; 3,604,299; 4,031,706; 4,104,950; 4,121,491; 4,132,141; 4,132,142; 4,135,428; 4,161,901, and other U.S. and foreign patents pending.
REVISIONS
A INC PER ECA 5608
B INC PER ECA 5690
C INC PER ECA 5645
D INC PER ECA 5682
E INC PER ECA 5704
F INC PER ECA 5778
G INC PER ECA 5940
REF
U2
C1
R19
Q2
Q1
R1
R4,R15, R16
D1
FS1
FS2
CR17, CR18
Q5, Q6
R20, R21
CR1-CR4 CR6, CR7 CR13, CR14
R14, R17
Q7, Q8
CR14, CR15, CR19, CR20
FS 3, FS4
TYP 8 PLACES
TYP 4 PLACES
J1
J6
J5
J4
J3
J2
RT2
RT1
RV1
SOFT
SUST
FS3 1A 250V
FS4 1A 250V
FS1 12A 250V
FS2 6A 250V
E1
E2
E3
E4
E5
E6
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICAL STANDARDS.
3. REFERENCE DRAWINGS:
SCHEMATIC: 100-06D016
P.W. BOARD: 100-05D016
P.W. MASTER: 100-08D016
4. HALF TONE CIRCUIT SHOWN NEAR SIDE. FAR SIDE CIRCUITRY OMITTED FOR CLARITY OF VIEW.
5.
6 TORQUE SCREW AND NUT MOUNTING TRANSISTOR TO 3.25 ± 0.25 IN. LBS.
BEF
NYLON SHOULDER WASHER SWS-411
#4 NUT
#4 LOCK WASHER SPLIT RING
FLAT WASHER, NYLON
FLAT WASHER #4
#4-40 x 3/8 LG, SCREW
BRACKET
INSULATOR, SILICONE RUBBER
SECTION A-A
4 PLACES
100-04D016-1 SHOWN
APPROVED FOR: PRODUCTION, PRE-PRODUCTION, PROTOTYPE
DATE
APPROVED
SUPERSCOPE CHATSWORTH, CALIFORNIA
PRINTED WIRING BOARD ASS'Y
SERIES-PASS POWER SUPPLY
D 26687 100-04D016 G

FIGURE 13B



REVISIONS

SYM.	DESCRIPTION	DFTMN	DATE	APPR'D.

ITEM	PART NO.	DESCRIPTION	REQ'D. PER ASSY.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
1. BREAK ALL SHARP CORNERS .015 MAX.
2. SURFACE ROUGHNESS 63 MICROINCH R.M.S. MAX.
3. DIAMETERS TO BE CONCENTRIC WITHIN .005 T.I.R.
4. FILLET RADIUS .010 MAX.
5. THREADS - CLASS 2

TOLERANCES UNLESS OTHERWISE NOTED
ANGLES ± 0° 30'
FRACTIONS ± 1/32
DECIMALS .XX ± .030, .XXX ± .010

DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

DRAWN BY: Marlyn Morgan DATE: 10-13-78
CHECKED
APPROVED
PROJ. ENG.

MATERIAL
FINISH

DASH NO. | NEXT ASSY. | MODEL NO.
APPLICATION

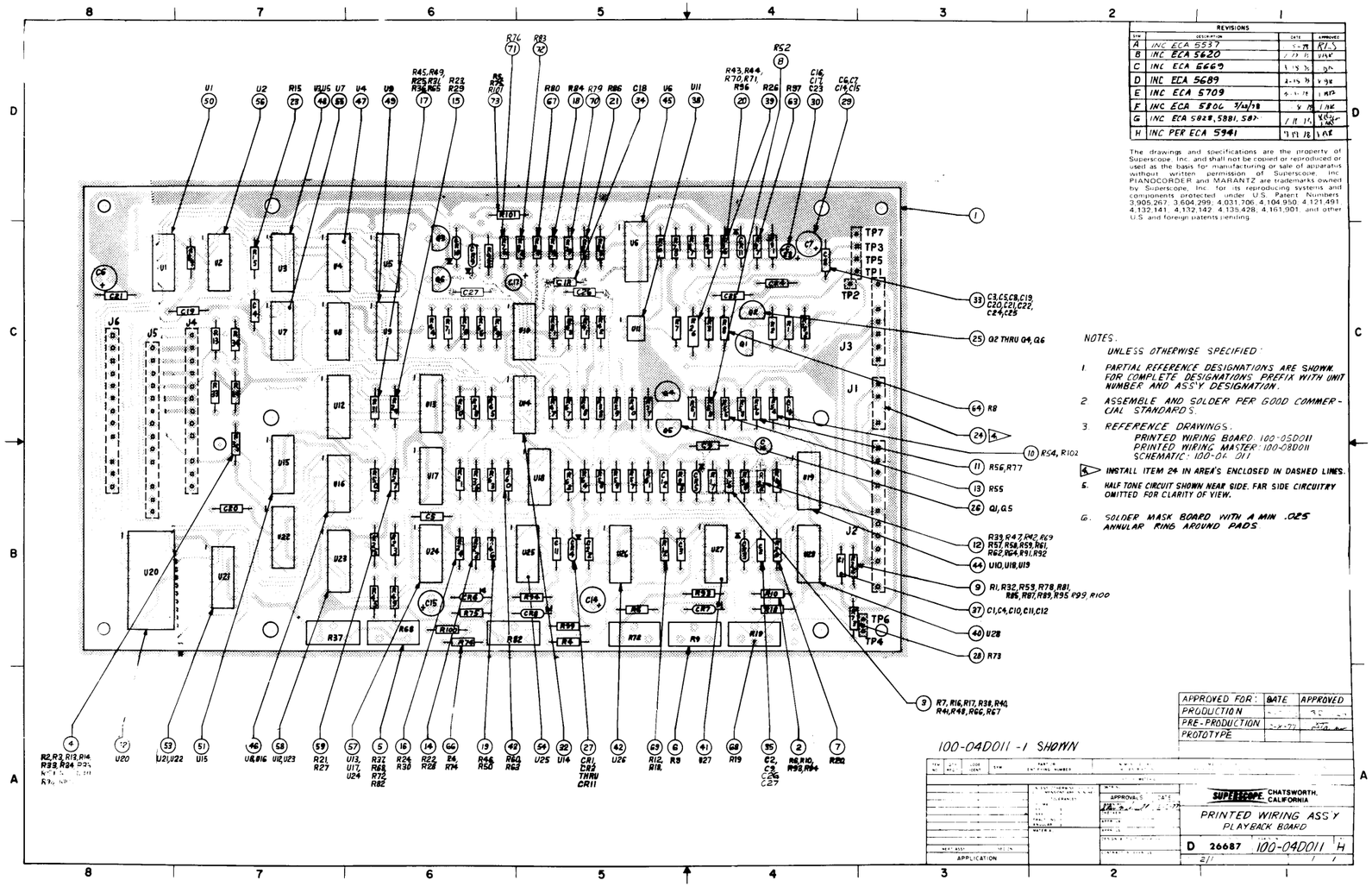
SUPERSCOPE CHATSWORTH CALIFORNIA

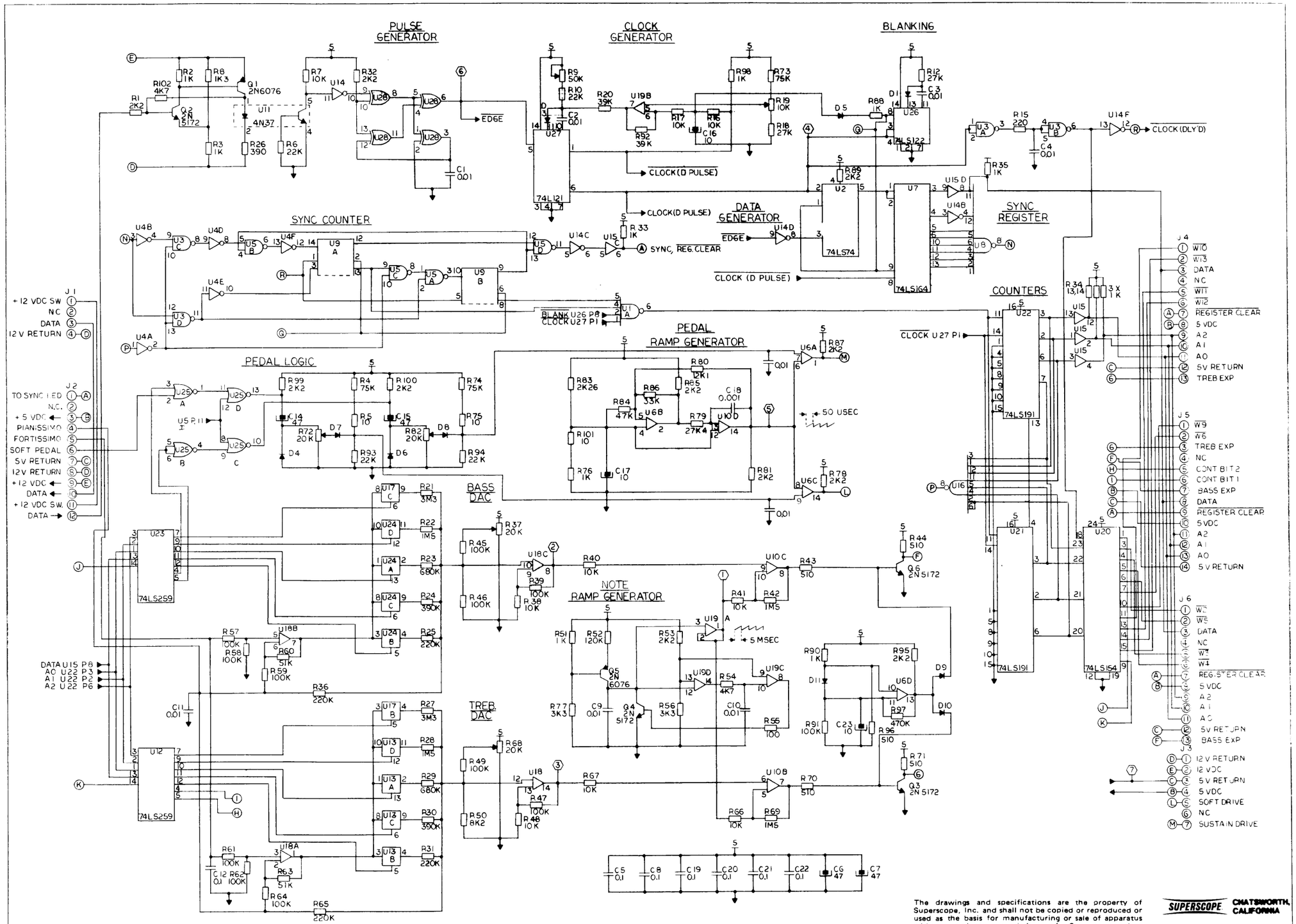
DWG. TITLE
POWER SUPPLY, PEDAL DRIVERS

RELATED DWGS. | DWG NO. | REV.
SCALE | SHEET OF

SS-MAR 0169

FIGURE 14-A


REVISIONS
The drawings and specifications are the property of Superscope, Inc. and shall not be copied or reproduced or used as the basis for manufacturing or sale of apparatus without written permission of Superscope, Inc. PIANOCORDER and MARANTZ are trademarks owned by Superscope, Inc. for its reproducing systems and components protected under U.S. Patent Numbers 3,905,267, 3,604,299, 4,031,706, 4,104,950, 4,121,491, 4,132,141, 4,132,142, 4,135,428, 4,161,901, and other U.S. and foreign patents pending.
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASS'Y DESIGNATION.
2. ASSEMBLE AND SOLDER PER GOOD COMMERCIAL STANDARDS.
3. REFERENCE DRAWINGS:
PRINTED WIRING BOARD: 100-05D011
PRINTED WIRING MASTER: 100-08D011
SCHEMATIC: 100-04 011
4. INSTALL ITEM 24 IN AREA'S ENCLOSED IN DASHED LINES.
5. HALF TONE CIRCUIT SHOWN NEAR SIDE. FAR SIDE CIRCUITRY OMITTED FOR CLARITY OF VIEW.
6. SOLDER MASK BOARD WITH A MIN .025 ANNULAR RING AROUND PADS
APPROVED FOR: PRODUCTION, PRE-PRODUCTION, PROTOTYPE
100-04D011 -1 SHOWN
SUPERSCOPE CHATSWORTH, CALIFORNIA
PRINTED WIRING ASS'Y
PLAYBACK BOARD
D 26687 100-04D011 H



⬡ TEST POINT
ALL DIODES IN914
ALL CAPACITORS IN MFD
NOTES: ALL RESISTORS IN OHMS

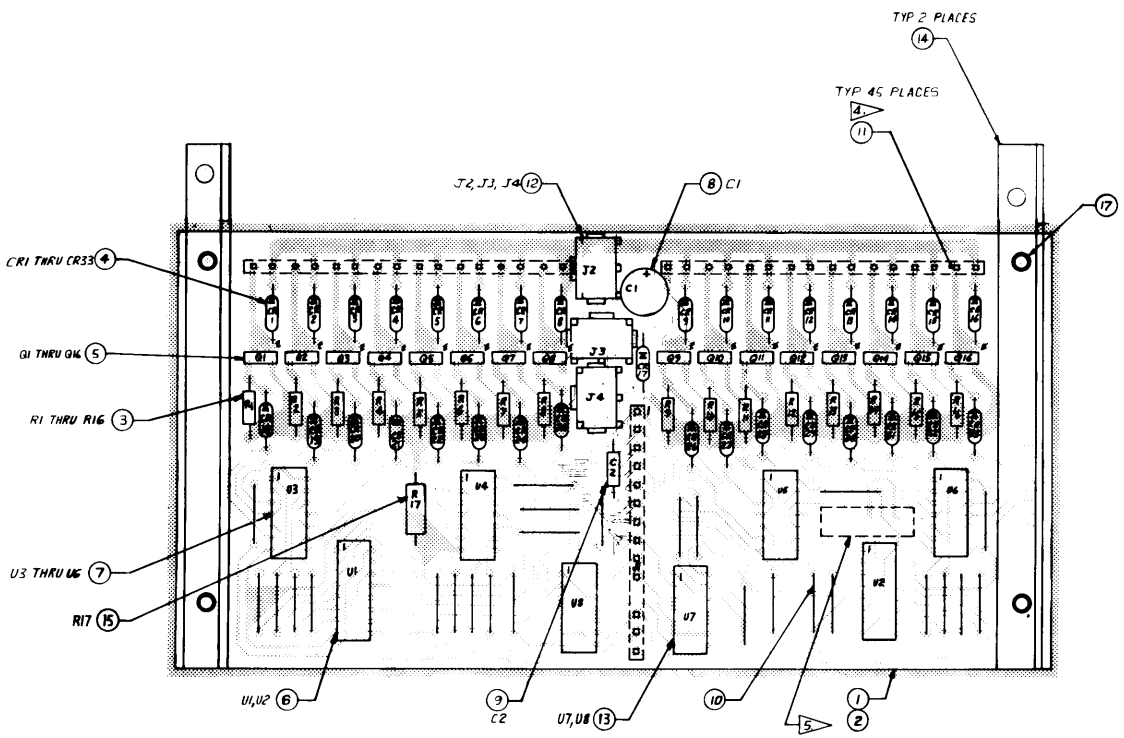
SUPERSCOPE CHATSWORTH, CALIFORNIA

DWG TITLE: PLAYBACK PC BOARD SCHEMATIC

RELATED DWGS | DWG NO | REV | SCALE | SHEET

FIGURE 15-A

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	INC PER ECA 5355	10/6/77	RLS
B	INC PER ECA 5389	11/9/77	RLS
C	INC PER ECA 5446	11/21/77	RLS
D	INC PER ECA 5564	1-28-78	JBR
E	INC PER ECA 5696	4-3-78	JBR



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLE AND SOLDER PER GOOD COMMERICIAL STANDARDS.
3. REFERENCE DRAWINGS:
   SCHEMATIC: 100-060004
   P.W. BOARD: 100-050004
   P.W. MASTER: 100-080004
   SILKSCREEN: 100-070004

4 INSTALL ITEM 11 IN ALL HOLES ENCLOSED INSIDE DASHED LINES

5 RUBBER STAMP REVISION LEVEL, DASH NO., AND DATE CODE IN APPROX. AREA SHOWN.

6 FOR (-1) ASSY SEE PL100-04D004-1
FOR (-3) ASSY SEE PL100-04D004-3
FOR (-5) ASSY SEE PL100-04D004-5

APPROVED FOR	DATE	APPROVED
PRODUCTION	1-28-78	JB RAMSEY
PRE-PRODUCTION	10/5/77	L E Godbey
PROTOTYPE		

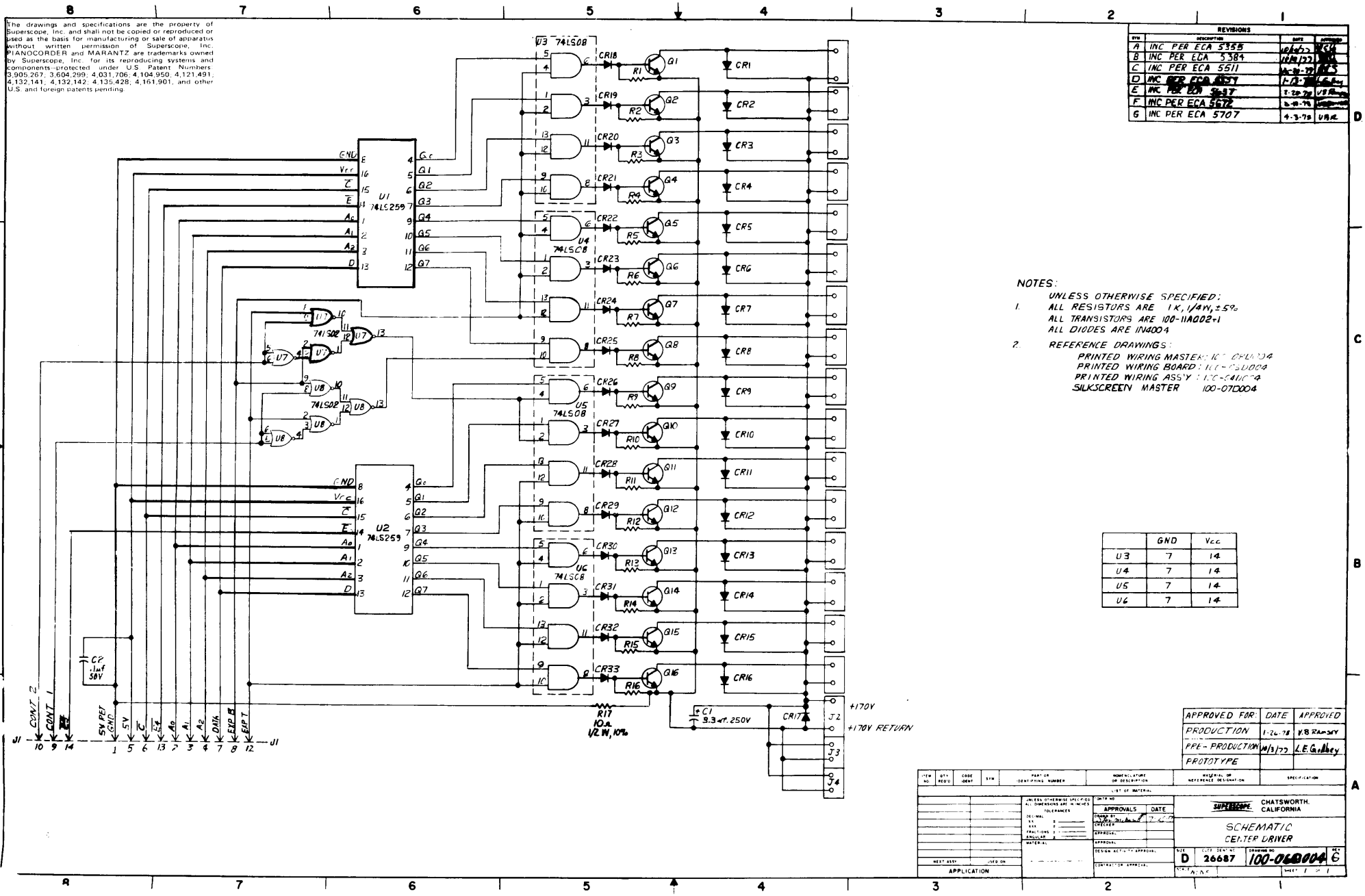
100-04D004-1 SHOWN 6

SUPERSCOPE CHATSWORTH, CALIFORNIA

PRINTED WIRING ASSEMBLY
CENTER DRIVER

D 26687 100-04D004 E

FIGURE 15-B



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	INC PER ECA 5355	10/6/77	[illegible]
B	INC PER ECA 5384	10/31/77	[illegible]
C	INC PER ECA 5511	1-20-78	[illegible]
D	INC PER ECA 5557	1-12-78	[illegible]
E	INC PER ECN 5637	2-20-78	[illegible]
F	INC PER ECA 5672	3-20-78	[illegible]
G	INC PER ECA 5707	4-3-78	[illegible]

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1K, 1/4W, ±5%
ALL TRANSISTORS ARE 100-11A002+1
ALL DIODES ARE IN4004
2. REFERENCE DRAWINGS:
PRINTED WIRING MASTER: 100-0[illegible]004
PRINTED WIRING BOARD: 100-0[illegible]004
PRINTED WIRING ASS'Y: 100-0[illegible]004
SILKSCREEN MASTER 100-070004

	GND	Vcc
U3	7	14
U4	7	14
U5	7	14
U6	7	14

APPROVED FOR	DATE	APPROVED
PRODUCTION	1-26-78	W.B. RAMSEY
PRE-PRODUCTION	10/3/77	L.E. Gadbey
PROTOTYPE		

ITEM NO	QTY REQ'D	CODE IDENT	SYM	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REFERENCE DESIGNATION	SPECIFICATION

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMAL
XX ±
XXX ±
FRACTIONS ±
ANGULAR ±
MATERIAL
NEXT ASSY | USED ON
APPLICATION

DATE NO
APPROVALS | DATE
DRAWN BY
CHECKER
APPROVAL
APPROVAL
DESIGN ACTIVITY APPROVAL
CONTRACTOR APPROVAL

SUPERSCOPE CHATSWORTH, CALIFORNIA

SCHEMATIC
CENTER DRIVER

SIZE D | CAGE IDENT NO 26687 | DRAWING NO 100-060004 | REV E
SCALE N.A.S. | SHEET 1 OF 1

FIGURE 16-A

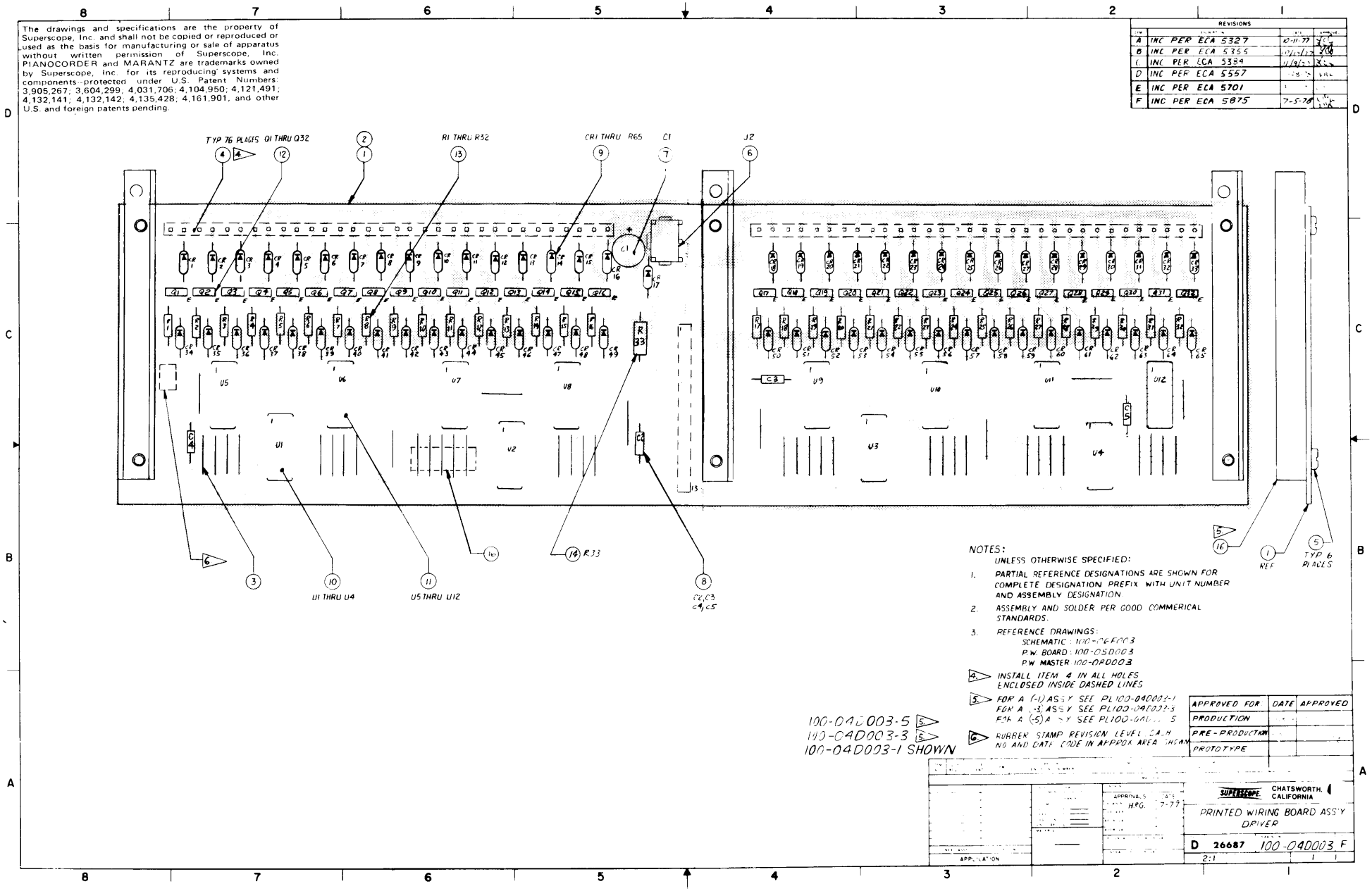

The drawings and specifications are the property of Superscope, Inc. and shall not be copied or reproduced or used as the basis for manufacturing or sale of apparatus without written permission of Superscope, Inc. PIANOCORDER and MARANTZ are trademarks owned by Superscope, Inc. for its reproducing systems and components protected under U.S. Patent Numbers: 3,905,267; 3,604,299; 4,031,706; 4,104,950; 4,121,491; 4,132,141; 4,132,142; 4,135,428; 4,161,901, and other U.S. and foreign patents pending.
REVISIONS
A INC PER ECA 5327 10-11-77
B INC PER ECA 5355
C INC PER ECA 5389
D INC PER ECA 5557
E INC PER ECA 5701
F INC PER ECA 5875 7-5-78
TYP 76 PLACES Q1 THRU Q32
R1 THRU R32
CR1 THRU R65
C1
J2
U1 THRU U4
U5 THRU U12
CR3 CR4 CR5
R33
TYP 6 PLACES
REF
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICAL STANDARDS.
3. REFERENCE DRAWINGS:
SCHEMATIC: 100-06F003
P.W. BOARD: 100-05D003
P.W MASTER 100-0RD003
4. INSTALL ITEM 4 IN ALL HOLES ENCLOSED INSIDE DASHED LINES.
5. FOR A (-1) ASSY SEE PL100-04D003-1
FOR A (-3) ASSY SEE PL100-04D003-3
FOR A (-5) ASSY SEE PL100-04D003-5
6. RUBBER STAMP REVISION LEVEL, SERIAL NO AND DATE CODE IN APPROX AREA SHOWN
100-04D003-5
100-04D003-3
100-04D003-1 SHOWN
APPROVED FOR PRODUCTION
DATE APPROVED
PRE-PRODUCTION
PROTOTYPE
APPLICATION
APPROVALS
MFG.
7-77
SUPERSCOPE CHATSWORTH, CALIFORNIA
PRINTED WIRING BOARD ASSY
DRIVER
D 26687 100-04D003 F
2:1

FIGURE 16-B

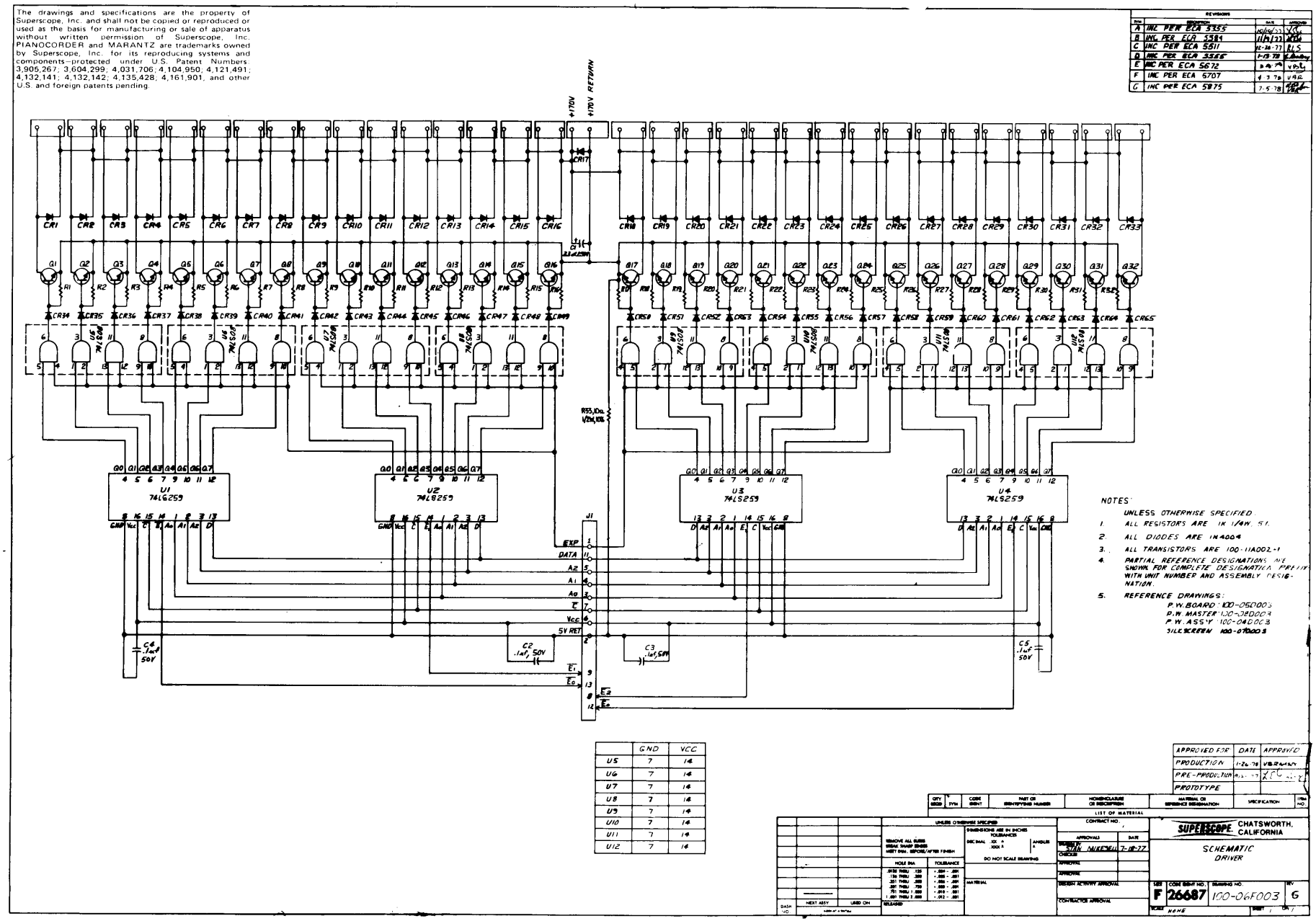
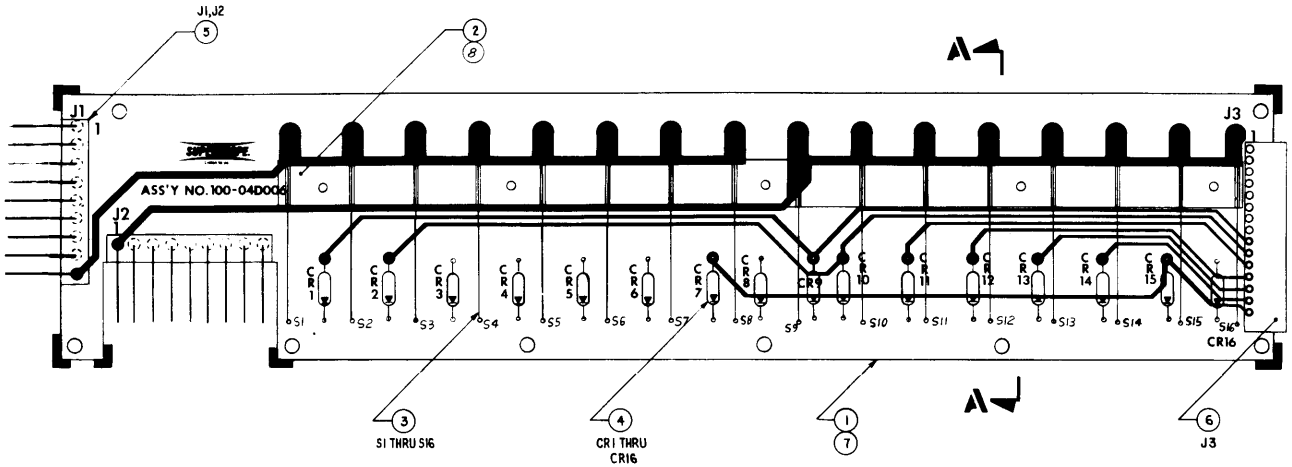
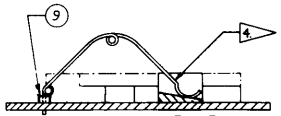

The drawings and specifications are the property of Superscope, Inc. and shall not be copied or reproduced or used as the basis for manufacturing or sale of apparatus without written permission of Superscope, Inc. PIANOCORDER and MARANTZ are trademarks owned by Superscope, Inc. for its reproducing systems and components—protected under U.S. Patent Numbers 3,905,267; 3,604,299; 4,031,706; 4,104,950; 4,121,491; 4,132,141; 4,132,142; 4,135,428; 4,161,901, and other U.S. and foreign patents pending.
REVISIONS
A INC PER ECA 5335
B INC PER ECA 5584
C INC PER ECA 5511
D INC PER ECA 5585
E INC PER ECA 5672
F INC PER ECA 5707
G INC PER ECA 5875
+17DV
+17DV RETURN
U1 74LS259
U2 74LS259
U3 74LS259
U4 74LS259
J1
EXP
DATA
A2
A1
A0
Vcc
5V RET
C2 .1uf, 50V
C3 .1uf, 50V
C4 .1uf 50V
C5 .1uf 50V
NOTES:
UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1K 1/4W, 5%.
2. ALL DIODES ARE 1N4004
3. ALL TRANSISTORS ARE 100-11A002-1
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
5. REFERENCE DRAWINGS:
P.W. BOARD: 100-05D003
P.W. MASTER: 100-07D003
P.W. ASS'Y: 100-04D003
SILKSCREEN: 100-07D003
GND VCC
U5 7 14
U6 7 14
U7 7 14
U8 7 14
U9 7 14
U10 7 14
U11 7 14
U12 7 14
APPROVED FOR DATE APPROVED
PRODUCTION 1-26-78
PRE-PRODUCTION
PROTOTYPE
LIST OF MATERIAL
SUPERSCOPE CHATSWORTH, CALIFORNIA
SCHEMATIC
DRIVER
F 26687 100-06F003 G
SCALE NONE

FIGURE 17

REVISIONS			
A	INC PER ECA 5380 DTP	11-1	
B	INC PER ECA 5471		
C	INC ECA 5574		
D	INC ECA 5666	3-9-78	
E	INC PER ECA 5678		
F	INC PER ECA 5946		





NOTES:
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICIAL STANDARDS.
3. REFERENCE DRAWINGS:
   SCHEMATIC - 100-06D005
   P.W. BOARD : 100-05D006
   P.W. MASTER: 100-08D006

4. AFTER SOLDERING ADJUST SWITCH TO POSITION SHOWN IN SECTION A-A. ITEM 9 IS WATER SOLUBLE AND IS DISOLVED AFTER SOLDERING IN CLEANING PROCESS

APPROVED FOR	DATE	APPROVED
PRODUCTION		
PRE PRODUCTION		
PROTOTYPE		

100-09D006-1 SHOWN

APPROVALS HMG. DATE 8-77

SUPERSCOPE CHATSWORTH, CALIFORNIA

PRINTED WIRING ASSEMBLY
KEY SWITCH (16)

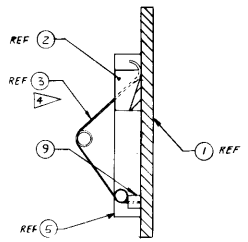
D 26687 100-09D006 F

2:1

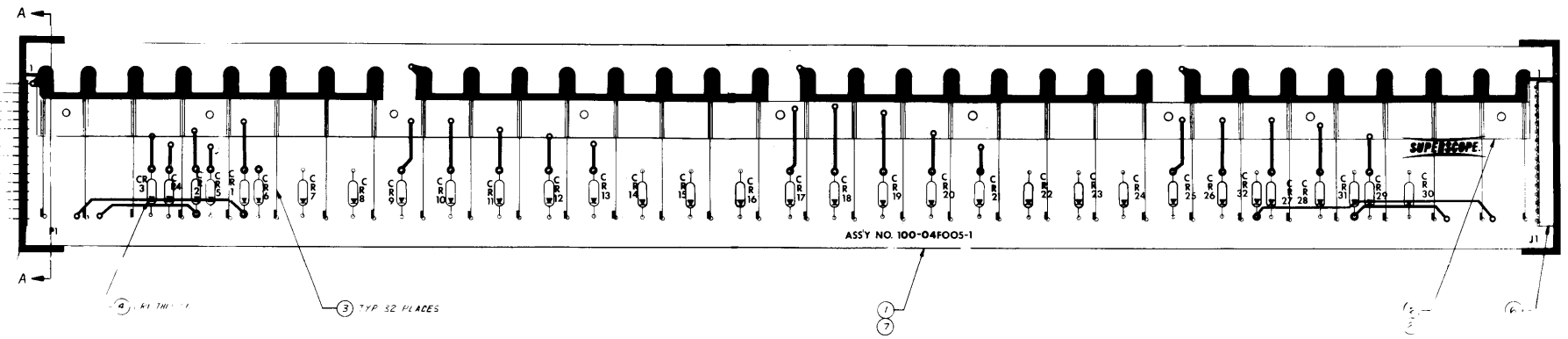
APPLICATION

FIGURE 18

REVISIONS			
LTR	DESCRIPTION	DATE	
A	INC PER ECA 5390 DNP	11/3/77	
B	INC PER ECA 5476	12/5/77	
C	INC PER ECA 5576	1-20-78	
D	INC PER ECA 5666	3-9-78	
E	INC PER ECA 5684	3-15-78	
F	INC PER ECA 5954	5-14-78	



SECTION A-A



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLE AND SOLDER PER GOOD COMMERICAL STANDARDS
3. REFERENCE DRAWINGS:
   SCHEMATIC 100-05D005
   P.W. BOARD 100-05F005
   P.W. MASTER 100-09F005
4. AFTER SOLDERING ADJUST SWITCH TO POSITION SHOWN IN SECTION A-A, ITEM 9 IS WATER SOLUBLE AND IS DISOLVED AFTER SOLDERING IN CLEANING PROCESS

100-04F005-1 SHOWN

APPROVED FOR	DATE APPROVED
PRODUCTION	
PRE-PRODUCTION	
PROTOTYPE	

SUPERSCOPE. CHATSWORTH, CALIFORNIA

PRINTED WIRING BOARD ASSY
32 KEY SWITCH

8-21-77

SIZE F | CODE IDENT NO. 26687 | DRAWING NO. 100-04F005 | F

SCALE 2/1 | SHEET 1

FIGURE 19

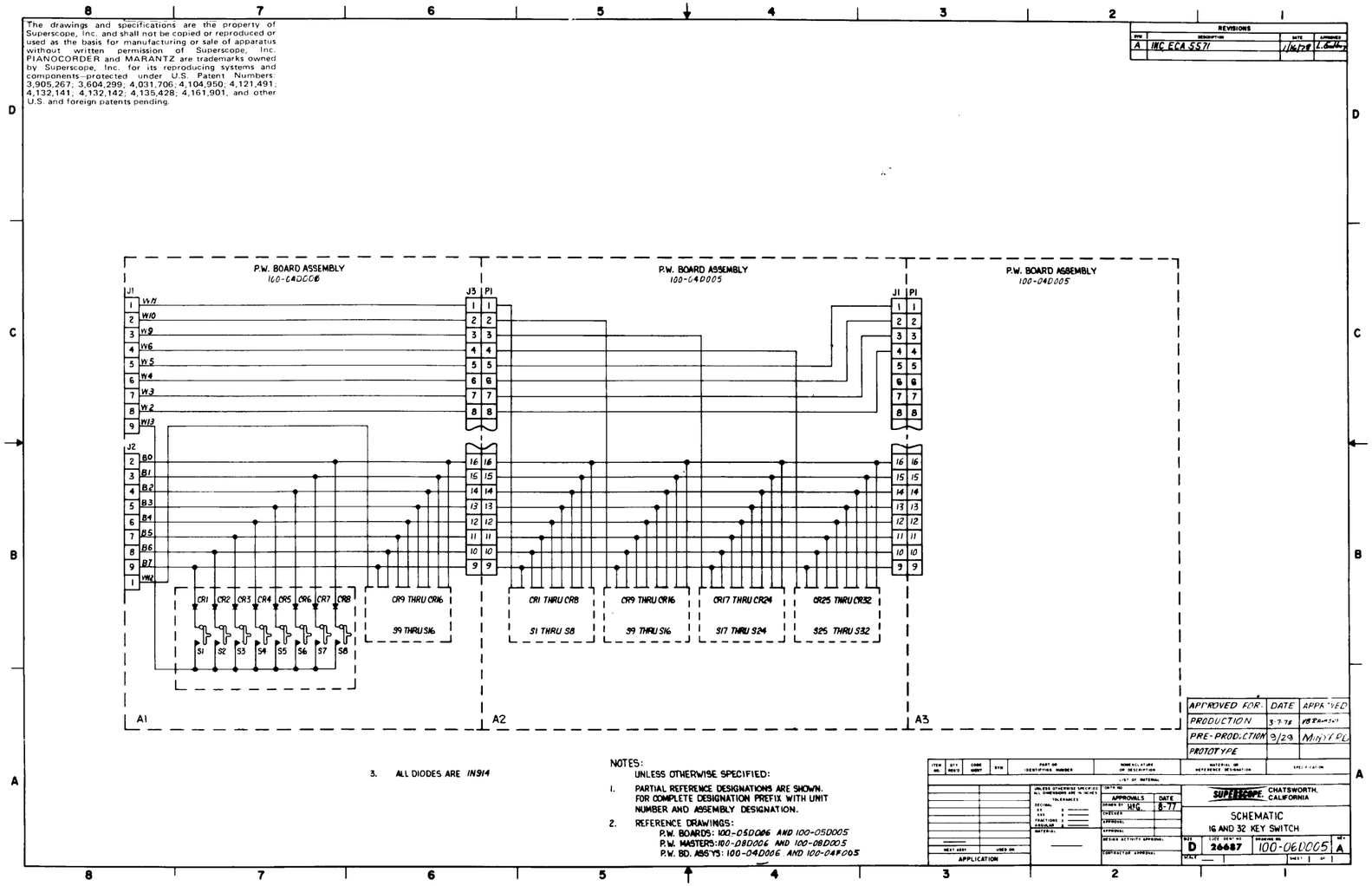
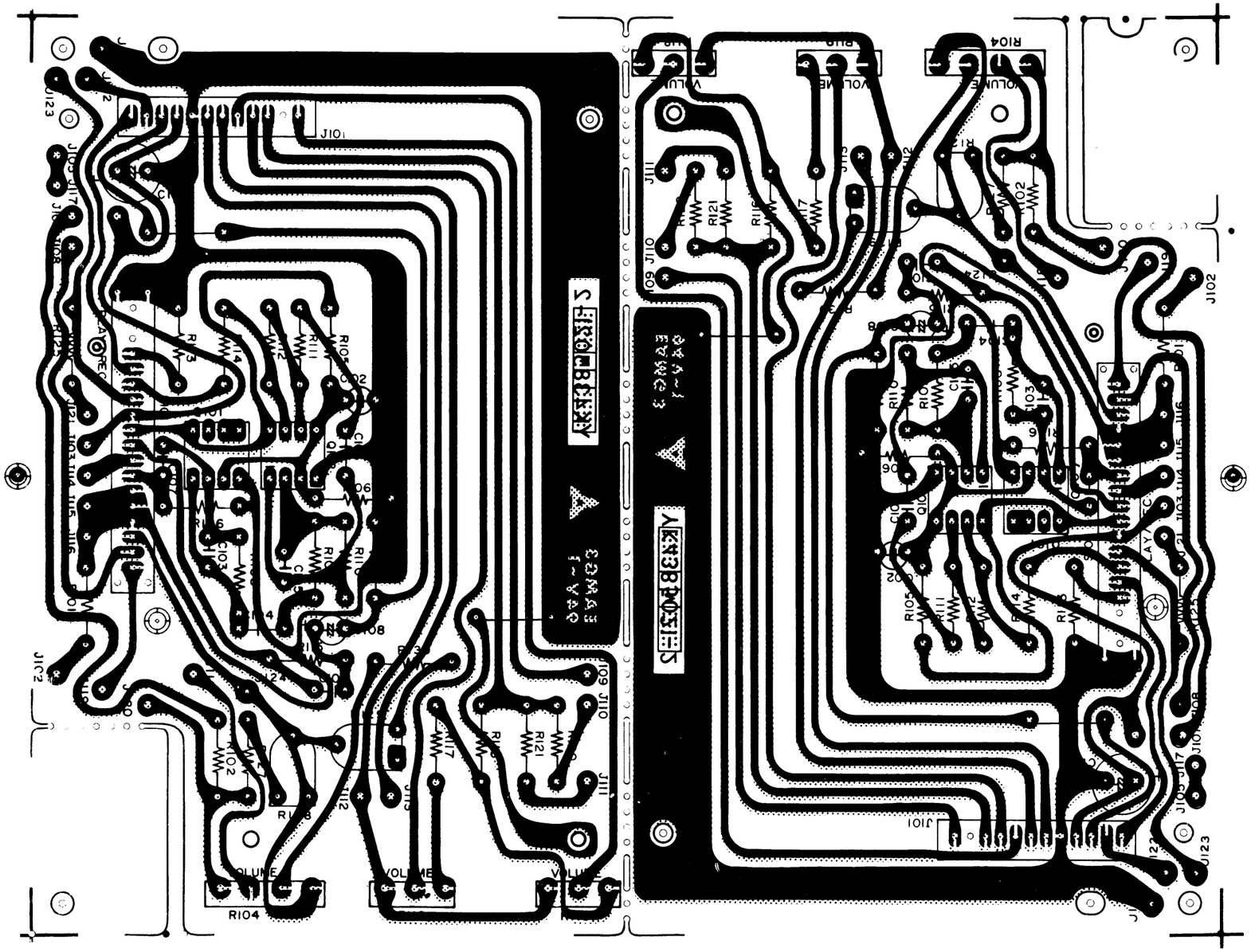

The drawings and specifications are the property of Superscope, Inc. and shall not be copied or reproduced or used as the basis for manufacturing or sale of apparatus without written permission of Superscope, Inc. PIANOCORDER and MARANTZ are trademarks owned by Superscope, Inc. for its reproducing systems and components-protected under U.S. Patent Numbers: 3,905,267; 3,604,299; 4,031,706; 4,104,950; 4,121,491; 4,132,141; 4,132,142; 4,135,428; 4,161,901, and other U.S. and foreign patents pending.
REVISIONS
A IHC ECA 5571 11/16/78
P.W. BOARD ASSEMBLY 100-04D006
P.W. BOARD ASSEMBLY 100-04D005
P.W. BOARD ASSEMBLY 100-04D005
J1 W11 W10 W9 W6 W5 W4 W3 W2 W13
J2 B0 B1 B2 B3 B4 B5 B6 B7 W12
J3 P1
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8
S1 S2 S3 S4 S5 S6 S7 S8
CR9 THRU CR16
S9 THRU S16
CR17 THRU CR24
S17 THRU S24
CR25 THRU CR32
S25 THRU S32
A1
A2
A3
3. ALL DIODES ARE IN914
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. REFERENCE DRAWINGS:
P.W. BOARDS: 100-05D006 AND 100-05D005
P.W. MASTERS: 100-08D006 AND 100-08D005
P.W. BD. ASSYS: 100-04D006 AND 100-04D005
APPROVED FOR PRODUCTION 3-7-78
PRE-PRODUCTION 3/29
PROTOTYPE
APPROVALS DRAWN BY HHG. DATE 8-77
SUPERSCOPE CHATSWORTH, CALIFORNIA
SCHEMATIC
16 AND 32 KEY SWITCH
SIZE D CODE IDENT NO 26687 DRAWING NO 100-06D005 REV A
SCALE —
SHEET 1 OF 1

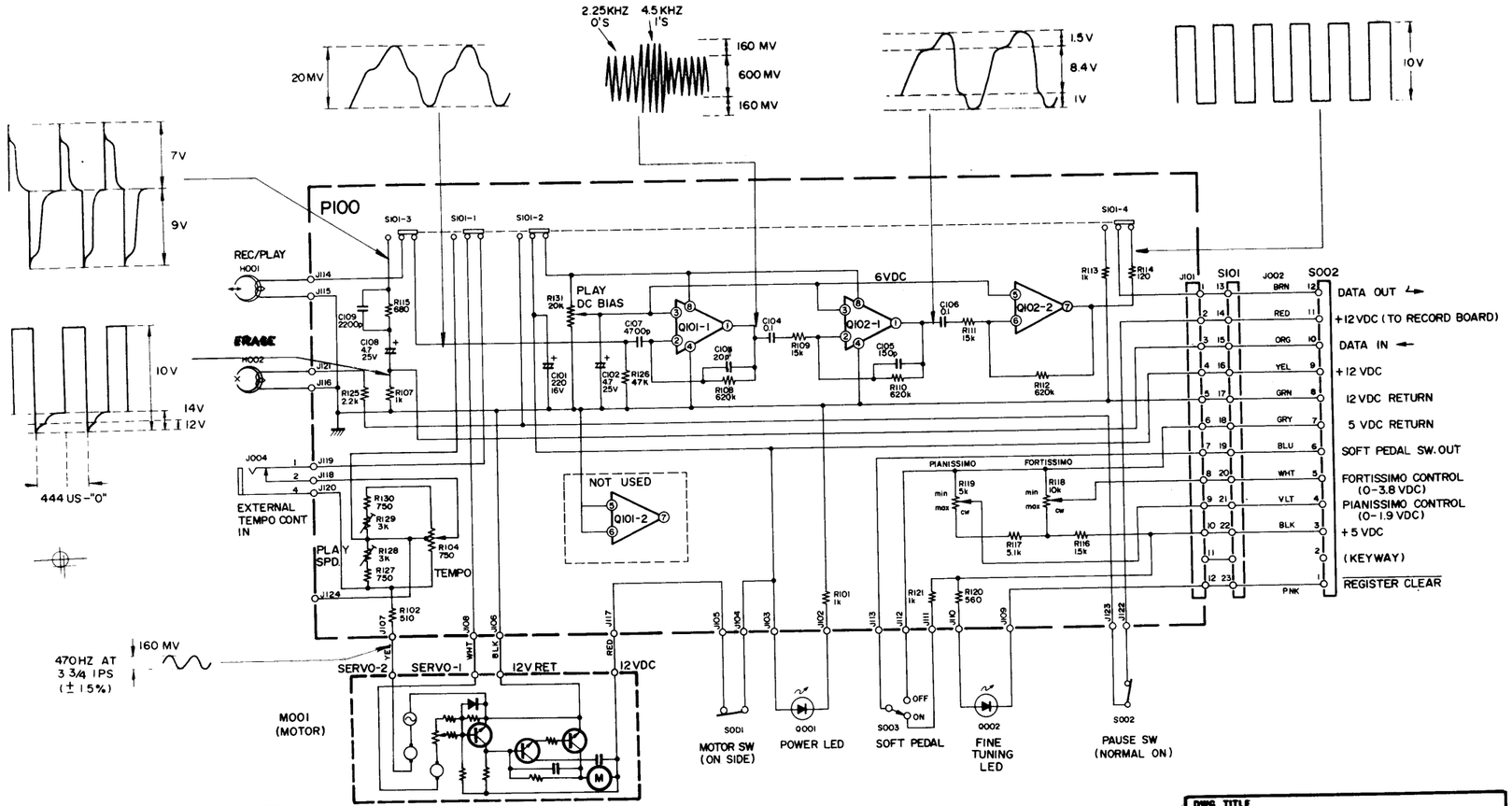
FIGURE 20



CHATSWORTH, CALIFORNIA

DWG. TITLE		
PT 100, CIRCUIT BOARD, W/COMPONENTS		
RELATED DWGS.	DWG. NO. 200-1077	REV.
	SCALE —	SHEET OF

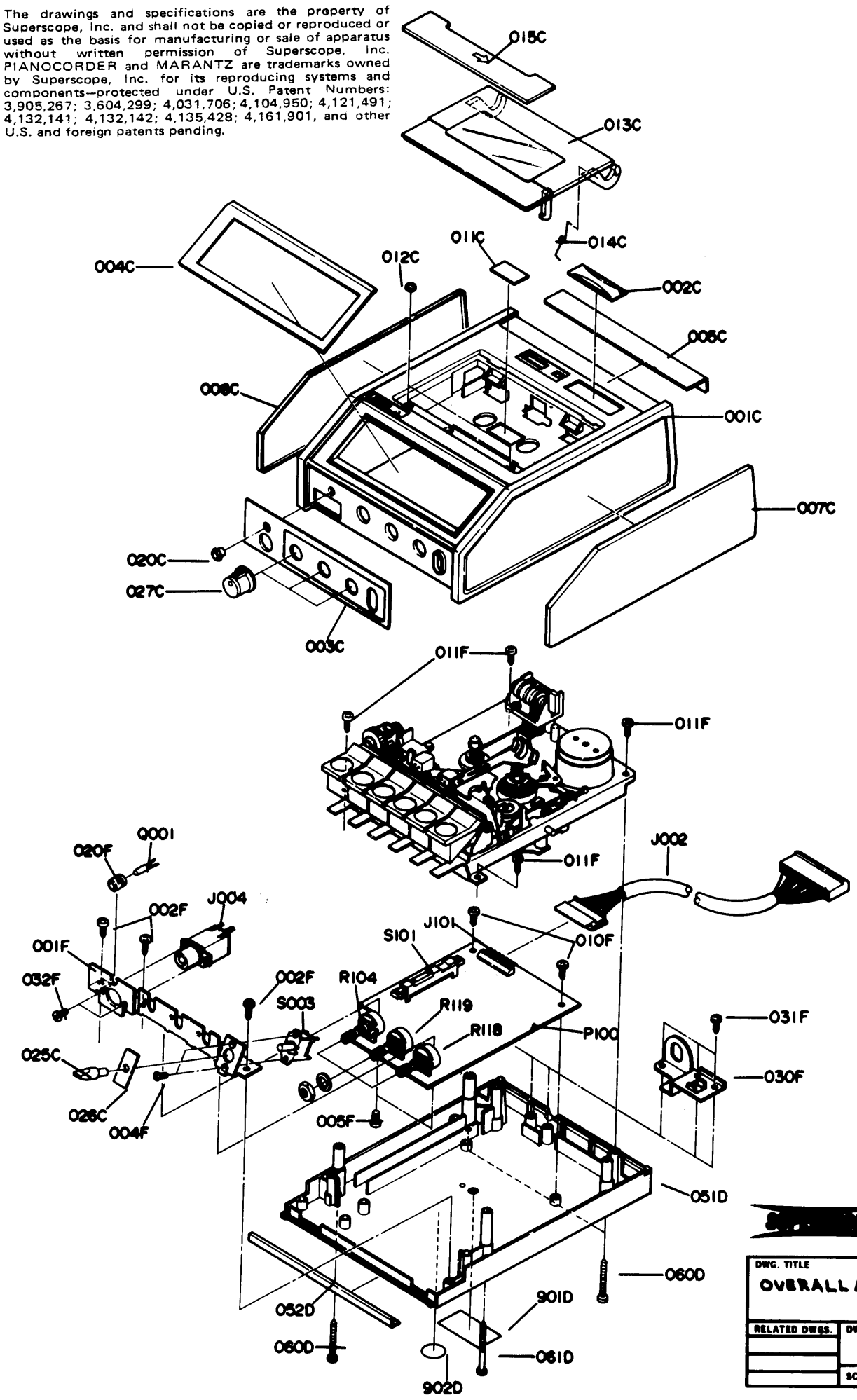
FIGURE 21



NOTE
1. S101 IS SHOWN PLAY BACK POSITION
2. ALL WIRES FROM RECORDER TO 48" LONG AND JACKETED
3. ALL RESISTORS ARE 1/4W ± 5%
4. Q101 AND Q102 ARE 4558D (JRC)
5. ALL PLAYBACK VOLTAGES AT 3 3/4 IPS

DWG. TITLE
SCHEMATIC PT 100

RELATED DWGS.	DWG NO. 100 1129	REV.
	SCALE	SHEET OF

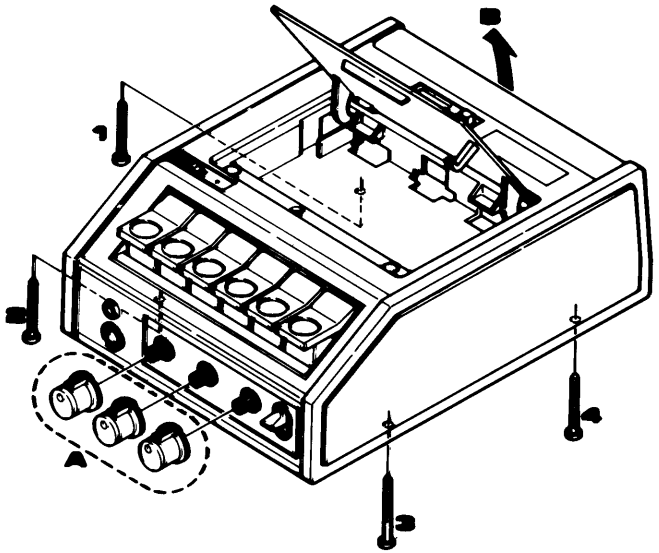


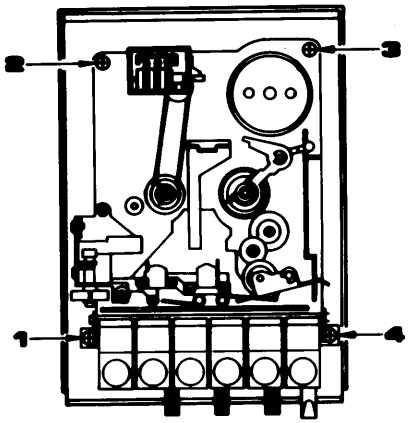
CHATSWORTH, CALIFORNIA

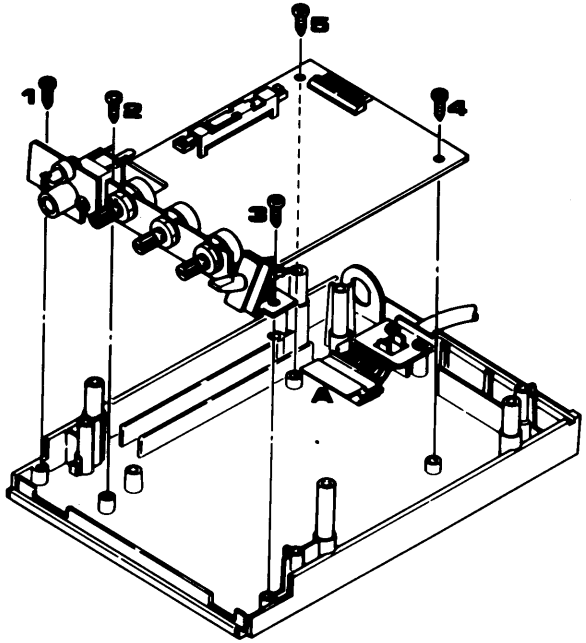
DWG. TITLE		
OVERALL ASSEMBLY		
RELATED DWGS.	DWG. NO. 217-1011	REV.
	SCALE —	SHEET 1 OF 1

FIGURE 22

FIGURE 23



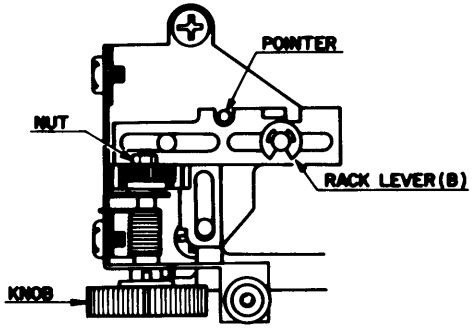


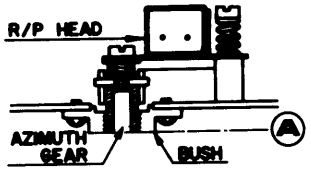


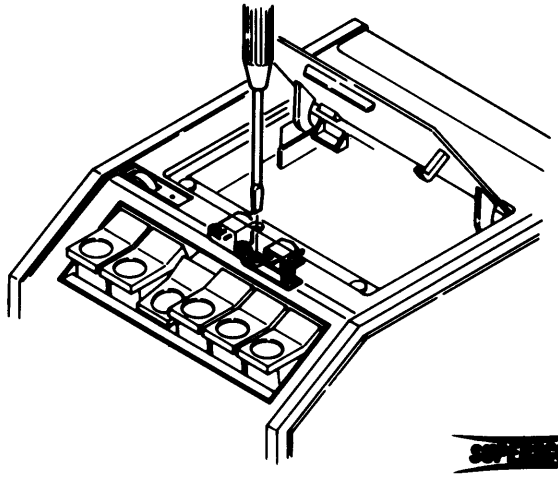
CHATSWORTH, CALIFORNIA

DWG. TITLE: ASSEMBLY		
RELATED DWGS	DWG. NO: 217-1009	REV.
	SCALE —	SHEET 1 OF 2

FIGURE 24



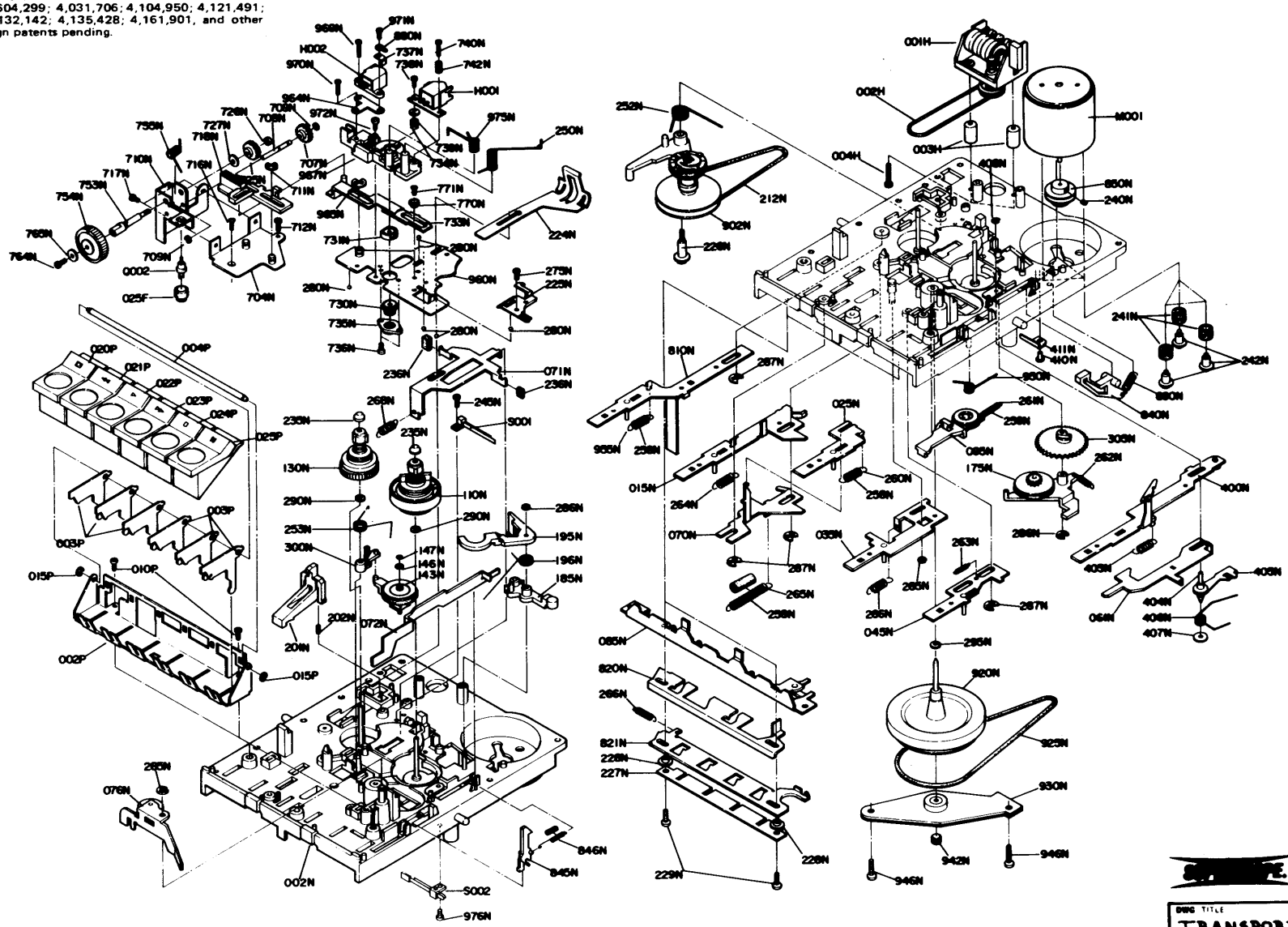




CHATSWORTH, CALIFORNIA

DWG. TITLE		
PT 100, AZIMUTH ADJUSTMENT		
RELATED DWGS.	DWG. NO. 217-1009	REV.
	SCALE —	SHEET 2 OF 2

FIGURE 25



CHATSWORTH, CALIFORNIA

DWG TITLE: TRANSPORT		
RELATED DWGS	DWG NO: 217-1010	REV.
	SCALE —	SHEET 1 OF 1

REV	S.C.N.	CHANGE
A		ADD R11 Q2-15 TO Q11-2
B		11-82 DEFINED SPECIAL MESSAGE EPROM ADDED C15

DATA BUS

ADDRESS BUS

XTAL 4MHZ

Q1 Z80A CPU

Q2 Z80A PIO

Q3 2716

Q4 2114-2

Q5 2114-2

Q10 2716 SPECIAL MESSAGE EPROM

Q6 7493 4BIT CNTR

Q7 74LS161 4BIT CNTR

Q8 74LS161 4BIT CNTR

Q9A Q9B Q9C Q9D 7404

Q9&Q11

Q11C Q11D Q11E 7414

Q12A Q12B Q12C Q12D 74LS86

Q13A Q13B 74LS74

Q14 74LS139

P1 DATA INPUT

P2

P3 OUTPUT

P4

TO Q12-6

TO Q11-2

TO Q13-13

TO Q2-15

P 14 + 5V
P 7 GND

NOTES

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS IN OHMS, 1/4W, 5%
   ALL CAPACITORS IN MFD
   ALL DIODES IN4004
2. ○ TEST POINT
3. REFERENCE DRAWINGS:
   PRINTED WIRING ASSY: 300-04D-001
   PRINTED WIRING BOARD: 300-05C-001
   SILKSCREEN MASTER: 300-07C-001
   PRINTED WIRING MASTER: 300-08D-001

RELATED DOCS	FIRST USED	DRAWN	DW 4-82
SAMPLES FROM THIS PRINT MUST BE SUBMITTED FOR APPROVAL PRIOR TO PRODUCTION		CHK	
DO NOT SCALE DRAWING		APPV	

marantz
CHATSWORTH CALIFORNIA

DISPLAY INTERFACE SCHEMATIC

300 - 06D - 001

SCALE | SH 1 OF 1

REV	E.C.N.	CHANGE
A		ADD JUMPER OPTION REMOVED R35 & U23 P10,11 CHANGED Q1-Q7 ADD J4
B		ADD PIEZO INDICATOR ADD 470Ω POT
C		DEFINED JUMPER OPTION

NOTES
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS IN OHMS, 1/4W, 5%
   ALL CAPACITORS IN MFD
   ALL DIODES IN4004
2. ○ TEST POINT
3. REFERENCE DRAWINGS:
   PRINTED WIRING ASSY: 300-04D-002
   PRINTED WIRING BOARD: 300-05C-002
   SILKSCREEN MASTER: 300-07C-002
   PRINTED WIRING MASTER: 300-06D-002

QTY	PART NO.	DESCRIPTION
		LIST OF MATERIAL

RELATED DOCS | FIRST USED

UNLESS OTHERWISE SPECIFIED:
1. BREAK ALL SHARP CORNERS .005 MAX
2. SURFACE ROUGHNESS 63 / MAX
3. DIMENSIONS TO BE ASSEMBLY WITH .005 T.I.R.
4. PALLET MARKING OPTIONAL
5. THREADS CLASS 2

DRAWINGS FINISH THIS PRINT MUST BE SUBMITTED FOR APPROVAL PRIOR TO PRODUCTION

DO NOT SCALE DRAWING

DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
FRACT ±1/32 ANGLES ±1° DEC .XX ± .020 .XXX ± .010

DRWN DW 5-82
CHK
P.E.
APPV

MARANTZ
CHATSWORTH CALIFORNIA

DISPLAY DRIVER BOARD
SCHEMATIC

300 - 06D - 002

SCALE | SH 1 OF 1

Pianocorder™*

Reproducing System

THIS MANUAL IS INTENDED ONLY AS A GUIDE TO THE TECHNICIAN IN HELPING HIM/HER UNDERSTAND THE OPERATION OF THE PIANOCORDER$_{TM}$ REPRODUCING SYSTEM/MARANTZ REPRODUCING PIANO. SUPERSCOPE, INC. RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

SUPERSCOPE®

20525 Nordhoff St. Chatsworth, Ca. 91311

PART NO. 199-1413-000
PRINTED IN U.S.A.